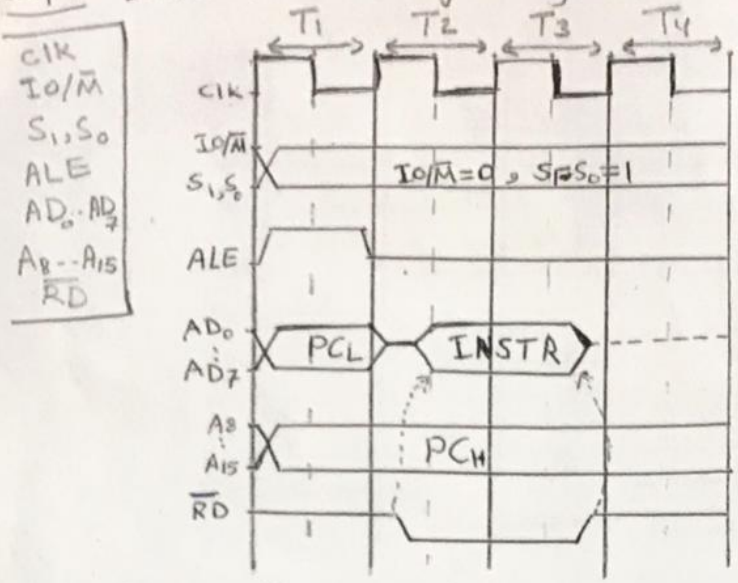
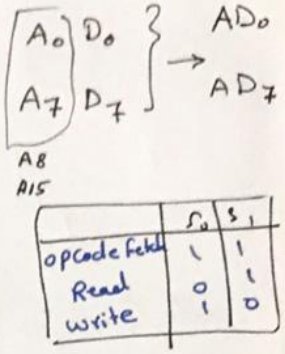
Microprocessor Architecture

Second Year
Dr. Rasha Thabit

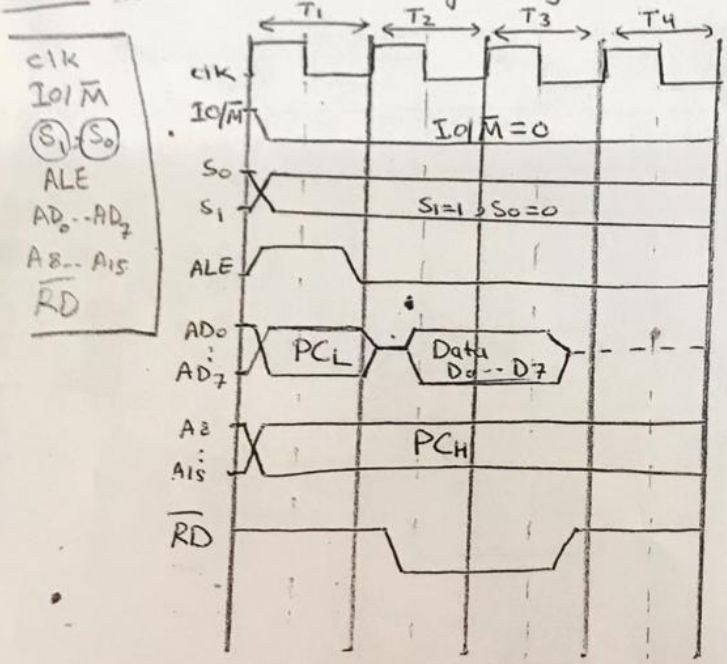
Q1 : Draw the timing diagram for opcode fetch



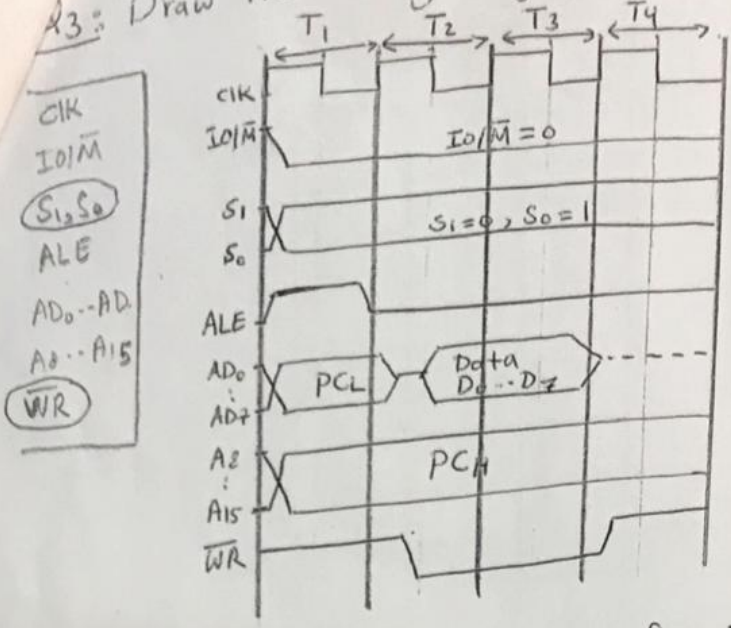


	S_0	S_1
opcode fetch	1	1
Read	0	1
write	1	0

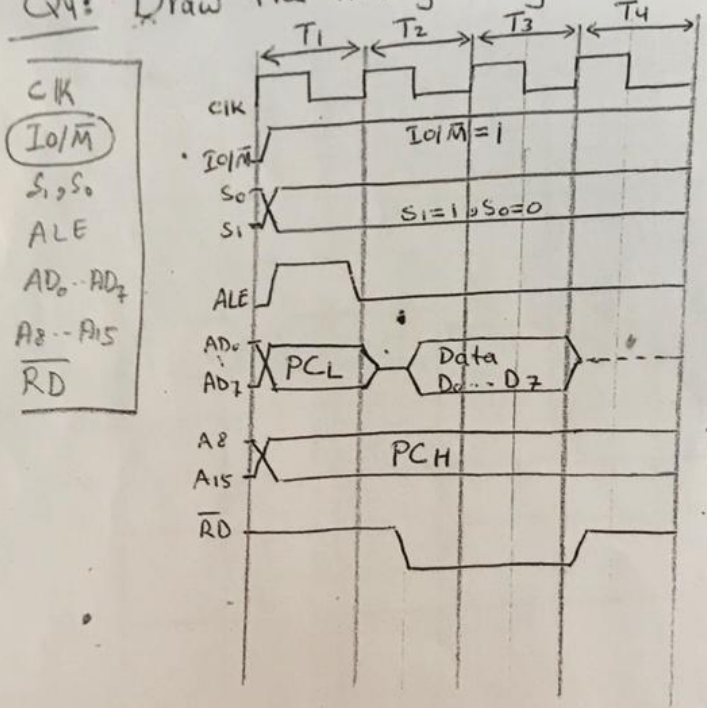
Q2 : Draw the timing diagram for Memory Read



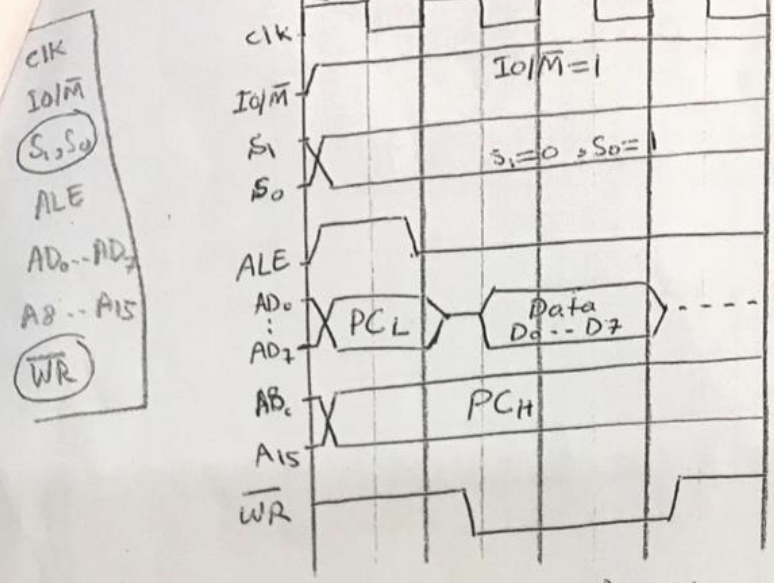
Q3: Draw the timing diagram for Memory Write



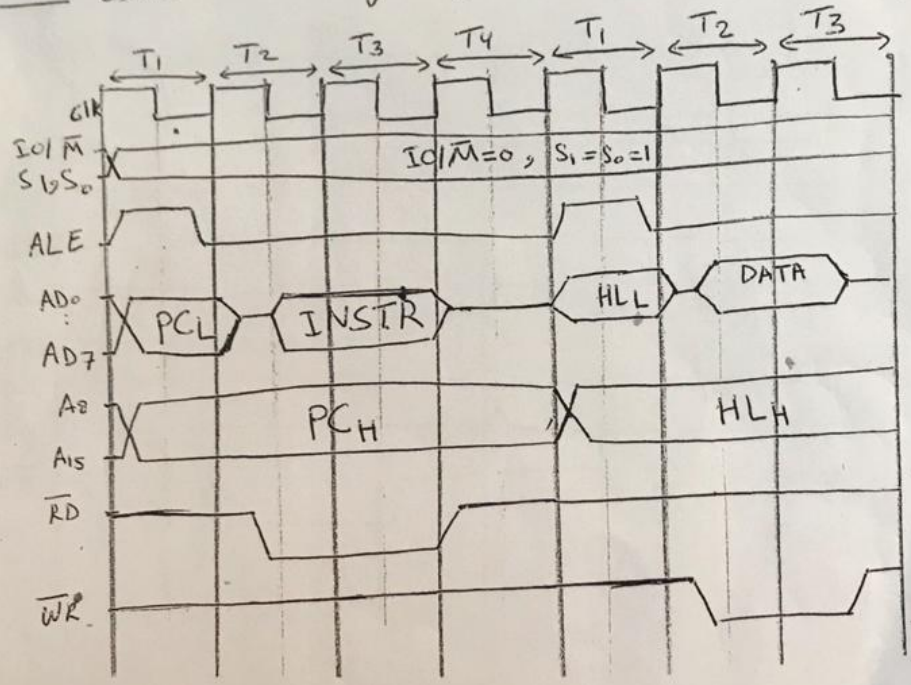
Q4: Draw the timing diagram for IORead



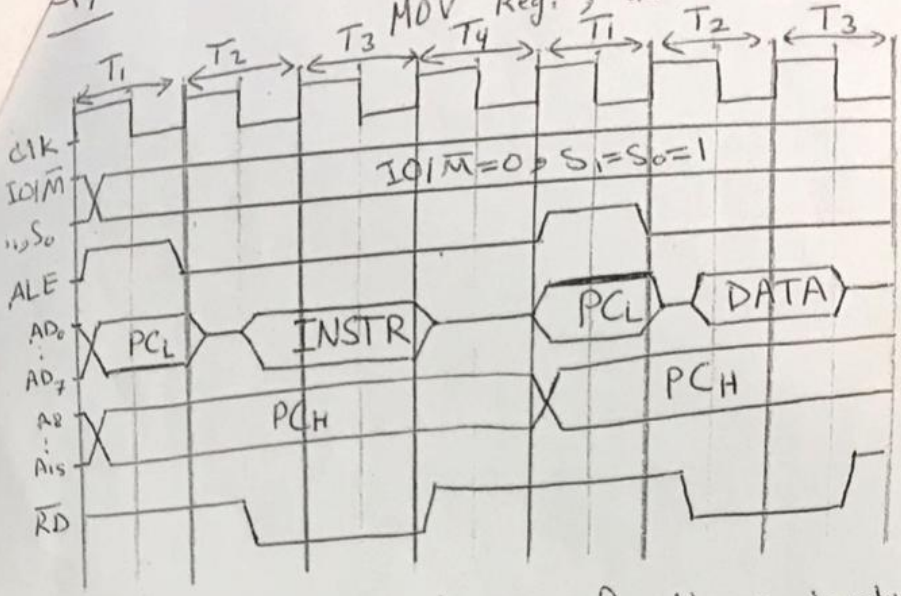
Q5: Draw the timing diagram for IO Write.



Q6: Draw the timing diagram for the instruction MOV M, reg
writting on memory



Q7: Draw the timing diagram for the instruction MOV reg, data
(MOV reg, d: Read from memory)



Q8: Draw the timing diagram for the instruction MOV reg2, reg