



Medical Instrumentations Techniques Engineering Al-Rasheed University College Second Level

# Digital Techniques

Lecture 06

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### LOGIC GATES TEST

This lecture explains the method of identifying the faulty logic gates followed by self-test questions that are related to the logic gates and logic circuits topics.

#### Lecture objectives

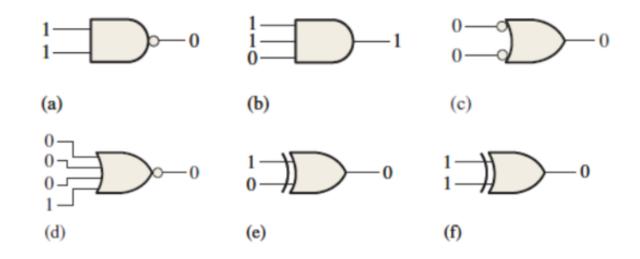
At the end of this lecture, the student should be able to:

- 1- Identify faulty logic gate in the logic circuit.
- Answer the self-test questions that are included in this lecture.

#### Identifying the faulty logic gate

The faulty logic gate is the one that gives wrong output. To identify the faulty logic gate, the right output must be determined and compared with the current output.

**Example:** Examine the following logic gates and identify the faulty logic gates.



	Right output	Current output	Gate status
а	$(\overline{1.1}) = \overline{1} = 0$	0	Active
b	(1.1.0) = 0	1	Faulty
с	$(\overline{0} + \overline{0}) = 1 + 1 = 1$	0	Faulty
d	$(\overline{0+0+0+1}) = \overline{1}$	0	Active
	= 0		
e	$1 \oplus 0 = 1$	0	Faulty
f	$1 \oplus 1 = 0$	0	Active

Self-Test

True or False

No.	Sentence	T or F
1	An inverter performs a NOT operation.	
2	A NOT gate cannot have more than one input.	
3	If any input to the OR gate is zero, the output is zero.	
4	If all the inputs to an AND gate are 1, the output is 0.	
5	A NAND gate can be considered as an OR gate followed by a NOT gate.	
6	A NOR gate can be considered as an OR gate followed by an inverter.	
7	The output of an EX-OR is 0 if the inputs are opposite.	
8	The output of an EX-NOR is 0 if the inputs are opposite.	
9	OR gate is considered faulty when the inputs are both zeros while the output is 1.	
10	The equation of AND gate output for two inputs A and B is (A+B).	

## Choose the correct answer:

1- When the input to an inverter is LOW (0), the output is		
(a) HIGH or 0		
(b) LOW or 0		
(c) HIGH or 1		
(d) LOW or 1		
2- An inverter performs an operation known as		
(a) Complementation		
(b) Assertion		
(c) Inversion		
(d) both answers (a) and (c)		

3- The output of an AND gate with inputs A, B and C is 0 (LOW) when ... (a) A = 0, B = 0, C = 0**(b)** A = 0, B = 1, C = 1(c) both answers (a) and (b) 4- The output of an OR gate with inputs A, B and C is 0 (LOW) when ... (a) A = 0, B = 0, C = 0**(b)** A = 0, B = 1, C = 1(c) both answers (a) and (b) 5- A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at t=0 and goes back LOW at t=1ms. The other pulse goes HIGH at t=0.8 ms and goes back LOW at *t*=3ms. The output pulse can be described as follows: (a) It goes LOW at t = 0 and back HIGH at t = 3 ms. (b) It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms. (c) It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms. (d) It goes LOW at t = 0.8 ms and back LOW at t = 1 ms.