Ministry of Higher Education & Scientific Research
Al-Rasheed University College
Department of Medical Laboratory Technique

وزارة التعليم العالي والبحث العلمي
كلية الرشيد الجامعة
قسم هندسة تقنيات الاجهزة الطبية

حقيبة تعليمية

بعنوان:
مكونات و دوائر الكترونية

إعداد

التدريسي الرئيسي: م.م دينا جمال جبار
التدريسي الثانوي: م.د سيف محمد براء

2023 - 2022

المقدمة

يتسم البرنامج التعليمي لمقرر الاجهزة والدوائر الالكترونية بالتدريس باللغة الانكليزية لمدة ثلاثون اسبوعا بواقع ساعتين نظري وثلاث ساعات عملي اسبوعيا يتم تدريس الطلبة باساسيات ومختلف التقنيات المتعلقة بالاجهزة والدوائر الالكترونية ضمن منهج متكامل ليتعرف الطالب على الدوائر الالكترونية وطرق تصميمها واستخدامها في تطبيقات عملية عديدة.

فهرس المحتويات

وصف المقرر الدراسي

يوفر وصف المقرر هذا إيجازاً مقتضياً لأهم خصائص المقرر ومخرجات التعلم المتوقعة من الطالب تحقيقها مبرهناً عما إذا كان قد حقق الاستفادة القصوى من فرص التعلم المتاحة. ولابد من الربط بينها وبين وصف البرنامج.؛

1. المؤسسة التعليمية	كلية الرشيد الجامعة
2. القسم العلمي / المركز	هندسة تقنيات الاجهزة الطبية
3. اسم / رمز المقرر	**مكونات ودوائر الكترونية**
4. أشكال الحضور المتاحة	**اسبوعيا 2 نظري و 3 عملي**
5. الفصل / السنة	سنوي
6. عدد الساعات الدراسية (الكلي)	**150 ساعة**
7. تاريخ إعداد هذا الوصف	1/9/2022
8. أهداف المقرر -تعريف الطالب بالدوائر الالكترونية الاساسية وطرق تصميمها واستخدامها وطرق تصميم بعض الدوائر -فهم ومعرفة التطبيقات العملية لديود والانترانسستر. - - فهم ومعرفة مضخمات الاشارة الكهربائية وانواعها. -التطبيقات العملية للمضخمات والدوائر الكهربائية المستخدمة	

9. مخرجات المقرر وطرائق التعليم والتعلم والتقييم
أ- الأهداف المعرفية ان يكون الطالب قادرا على ان - أ 1 التعرف على منحنى خصائص الاشارة الخارجة من الدايود والتطبيقات العملية التي تستخدم ييها. - أ 2 استخدام بعض الاجهزة المختبرية والتعرف على تطبيقاتها. - أ 3 تصميم بعض الدوائر الالكترونية.
ب - الأهداف المهار آتية الخاصة بالمقرر. ان يكون الطالب قادرا على ان: - ب 1 حساب القيم الداخلة والخارجة من الدوائر التي تحتوي على الدايود. – ب 2 استخدام بعض الاجهزة المختبرية والتعرف على تطبيقاتها – ب 3 تصميم بعض الدوائر الالكترونية
ج- الأهداف الوجدانية والقيمية ج1- يلتزم بأخلاقيات المؤسسة التعليمية ج2- يعمل بروح الفريق ج3- يستقبل ويتقبل المعرفة
طرائق التعليم والتعلم
1- محاضرات صفية 2- وسائل الايضاح (data show) 3- ورش عمل 4- مختبرات علمية 5- كتب ورقية والكترونية
طرائق التقييم
1- الامتحانات العملية 2- الامتحانات او التغذية الراجعة feed back 3- الواجبات البيتية 4- الحضور اليومي 5- تقارير مختبرية 6- الامتحانات الفصلية النهائية
د - المهارات العامة والتأهيلية المنقولة (المهارات الأخرى المتعلقة بقابلية التوظيف والتطور الشخصي). د1- مهارة الالقاء وابداء الراي في المحاضرة من خلال seminar د2- مهارة المناقشة في المحاضرة د3- مهارة حل المشكلات من خلال ورش العمل د4- زيادة قدرة الطالب على استخدام الاجهزة المختبرية.

10. بنية المقرر

الاسبوع	الساعات	المادة النظرية	طريقة التعليم	طريقة التقييم
2–1	10	Introduction to semiconductor materials and diode characteristics .	محاضرات صفية + data show	الواجبات البيتية
4–3	10	DC diode applications	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
6–5	10	AC diode applications	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
7	5	Zener diode characteristics and applications	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
10–9–8	15	BJT transistor characteristics	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
–12–11 13	15	DC analysis of BJT transistor	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
–15–14 17–16	20	AC analysis of BJT transistor	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
18-19-20-21	20	FET transistor characteristics and applications	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
23–22	10	Frequency response	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
–25–24 27–26	20	Operational Amplifiers and their applications	محاضرات صفية + data show	الامتحانات +الواجبات البيتية
–29–28 30	15	Power Amplifier	محاضرات صفية + data show	الامتحانات +الواجبات البيتية

10. البنية التحتية	
1- الكتب المقررة المطلوبة	Fundamentals of Electronics: Book 1: Electronic Devices and Circuit Applications Morgan & Claypool Publishers
2- المراجع الرئيسية (المصادر)	Electronic Devices and Circuit Applications Morgan & Claypool Publishers lectronic Devices and Circuit Theory (11th Edition Robert L. Boylestad, Louis Nashelsky
ا- الكتب والمراجع التي يوصى بها (المجلات العلمية , التقارير ,....)	الالي التحكم كتاب والالكترونية الكهربائية الدوائر تحليل كتاب وجيه جرجيس The art of Electronice
ب - المراجع الالكترونية, مواقع الانترنيت	

11. خطة تطوير المقرر الدراسي
سيتم تطوير المقرر من خلال ما يستجد من كتب وبحوث تتعلق بدوائر الالكترونية يي المستوعبات العلمية سكوباس وكلاريفيت

HIGHER EDUCATION PERFORMANCE REVIEW: PROGRAMME REVIEW

COURSE SPECIFICATION

This Course Specification provides a concise summary of the main features of the course and the learning outcomes that a typical student might reasonably be expected to achieve and demonstrate if he/she takes full advantage of the learning opportunities that are provided. It should be cross-referenced with the programme specification.

1. Teaching Institution	Electrical engineering technical colleges
2. University Department/Centre	Department of medical instrumentation engineering techniques
3. Course title/code	Electronic
4. Programme(s) to which it contributes	
5. Modes of Attendance offered	Theory , laboratory
6. Semester/Year	YEAR
7. Number of hours tuition (total)	150 hours (60 theory + 90 practice)
8. Date of production/revision of this specification	1/9/2022
9. Aims of the Course	
1. clarify the properties of electronic materials and how it is manufactured	
2. Understand and know the practical applications of diode and transistor	
3. Understand and know the types of transistors and the principle of each one's work	
4. Identify the electric signal amplifiers and their types	
5. Understand the practical applications of amplifiers and electrical circuit	

10- Learning Outcomes, Teaching ,Learning and Assessment Methode

A- Knowledge and Understanding

A1. Identify the characteristics of the curve of the output signal of the diode and the practical applications in which it is used

A2. Understand the transistor characteristics and identify the input and output signal of the transistor

A3. Become acquainted with different types of the transistor

A4. Become familiar with the frequency response of a BJT and FET amplifier.

A5. Understand the different types of operational amplifier, their applications and frequency response of their amplifiers

A6 . know the integrated circuits

B. Subject-specific skills

B1. Calculate the input and output values of the electronic circuits that contain the diode or transistor

B2. design circuits according to certain values

B3.

Teaching and Learning Methods

Academic lectures that contribute to establishing a strong foundation to support the cognitive ability of the student

practical laboratory, which provides practical experience to the student through practical experiments, which in turn support and promote the understanding and perception of the theoretical side

Assessment methods

Interactive assessment conducted directly between student and teacher is one of the feedback methods that faculty members depends on to evaluate the teaching and learning process

Periodic tests provides infomation on the extent to which student's follow-up the scientific content and the extent to which the given information can be understood

Quarterly tests and a middle course that held the student's interest and follow-up of the scientific material by its theoretical and skill during the entire semester

Final exams are the final seminar in the assessment of the student and interaction and interest in the scientific material during the whole academic year

C. Thinking Skills

C1. Creating creativity among students and find solutions to different problems
C2. Developing students' ability to work as team members with effective results
C3. Developing students' sense of responsibility and psychological preparation
C4. Develop the studiousness in accomplishing the work to reach satisfactory results

Teaching and Learning Methods

Motivate the creative side by posing various problems to students and urging them to find appropriate solutions
Forming work teams to assess the results of their work and change their structure periodically to develop the spirit of cooperation and development and motivate students to make intensive efforts to work different roles

Assessment methods

Direct assessment where the assessment is done by the teacher directly and write their observations about it
Practical projects and graduation projects and evaluate the student's ability to creativity, achievement and teamwork and ability to find solutions to various scientific problems

D. General and Transferable Skills (other skills relevant to employability and personal development)

D1. Calculate the input and output values of the electronic circuits that contain the diode or transistor
D2. How to design circuits according to certain values
D3. Know the analysis of any complex electronic circuit

11. Course Structure					
Week	Hours	ILOs	Unit/Module or Topic Title	Teaching Method	Assessment Method
1st-2nd	10	Introduction to semiconductor materials and diode characteristics	semiconductor materials	Lecture + practical	Oral test
3rd-4th	10	DC diode applications	Diode applications	Lecture + practical	Daily test
5th-6th	10	AC diode applications	Diode applications	Lecture + practical	Daily test
7th	5	Zener diode characteristics and applications	Zener diode	Lecture + practical	Daily test
8th-9th-10th	15	BJT transistor characteristics	BJT transistor	Lecture + practical	Daily test
11th-12th-13th	10	DC analysis of BJT transistor	DC analysis of BJT transistor	Lecture + practical	Daily test
14th-15th-16th-17th	20	AC analysis of BJT transistor	AC analysis of BJT transistor	Lecture + practical	First term exam
18th-19th-20th-21th	20	FET transistor characteristics and applications	FET transistor	Lecture + practical	Test
22th-23th	10	Frequency response	Frequency response	Lecture + practical	Second term exam
24th-25th-26th-28th	20	Operational Amplifiers and their applications	Operational Amplifiers	Lecture + practical	Test
28th-29th-30th	15	Power Amplifier	Power Amplifier	Lecture + practical	Final exam

12. Infrastructure	
Required reading: · CORE TEXTS · COURSE MATERIALS · OTHER	Electronic Devices and Circuit Theory Eleventh Edition Robert L. Boylestad Louis Nashelsky
Special requirements (include for example workshops, periodicals, IT software, websites)	
Community-based facilities (include for example, guest Lectures , internship , field studies)	

إرشادات للطلبة

- الرغبة والحماس للتعليم
- كن مشاركاً في جميع الأنشطة
- احترم أفكار المدرس والزملاء
- أنقد أفكار المدرس والزملاء بأدب إن كانت هناك حاجة.
- احرص على استثمار الوقت
- تقبل الدور الذي يسند إليك في المجموعة
- حفز أفراد مجموعتك في المشاركة في النشاطات
- احرص على بناء علاقات طيبة مع المدرس والزملاء أثناء المحاضرة
- احرص على ما تعلمته في المحاضرة وطبقه في الميدان .
- ركز ذهنك بالتعليم واحرص على التطبيق المباشر
- تغلق الموبايل قبل الشروع بالمحاضرة

الوحدة الأولى - المحاضرة الأولى - الزمن: 120 دقيقة

أهداف المحاضرة الاولى:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

1. **فهم ومعرفة المواد أشباه الموصلات**
2. **بعض من خصائص الدايود**

موضوعات المحاضرة الاولى:

.1definition of the Semiconductor Diodes
.2types of Semiconductor Diodes
.3basic operation and characteristics of a diode in

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التدريبية	الوسائل التدريبية
1	• نشاط التعارف • محاضرة • مناقشة • سؤال وجواب	• جهاز حاسوب • جهاز عرض • سبورة • اوراق واقلام

خطة إجراءات تنفيذ المحاضرة الاولى

الوحدة	المحاضرة	الإجراءات	الزمن بالدقيقة
الأولى	الأولى	الترحيب بالطلبة والتعارف معهم التعريف بالبرنامج وأهدافه وأهميته والبدء باعطاء المادة العلمية للمحاضرة	120 دقيقة

المادة العلمية:

1.1 SEMICONDUCTOR MATERIALS: Ge, Si, AND GaAs

The construction of every discrete (individual) solid-state (hard crystal structure) electronic device or integrated circuit begins with a semiconductor material of the highest quality.

Semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator.
In general, semiconductor materials fall into one of two classes: single-crystal and compound.
Single-crystal semiconductors such as germanium (Ge) and silicon (Si) have a repetitive crystal structure, whereas compound semiconductors such as gallium arsenide (GaAs), cadmium sulfide (CdS), gallium nitride (GaN), and gallium arsenide phosphide (GaAsP) are constructed of two or more semiconductor materials of different atomic structures.

1.2 COVALENT BONDINGAND INTRINSIC MATERIALS

The fundamental components of an atom are the electron, proton, and neutron. In the lattice structure, neutrons and protons form the nucleus and electrons appear in fixed orbits around the nucleus. The Bohr model for the three materials is provided in Fig. 1.3 .

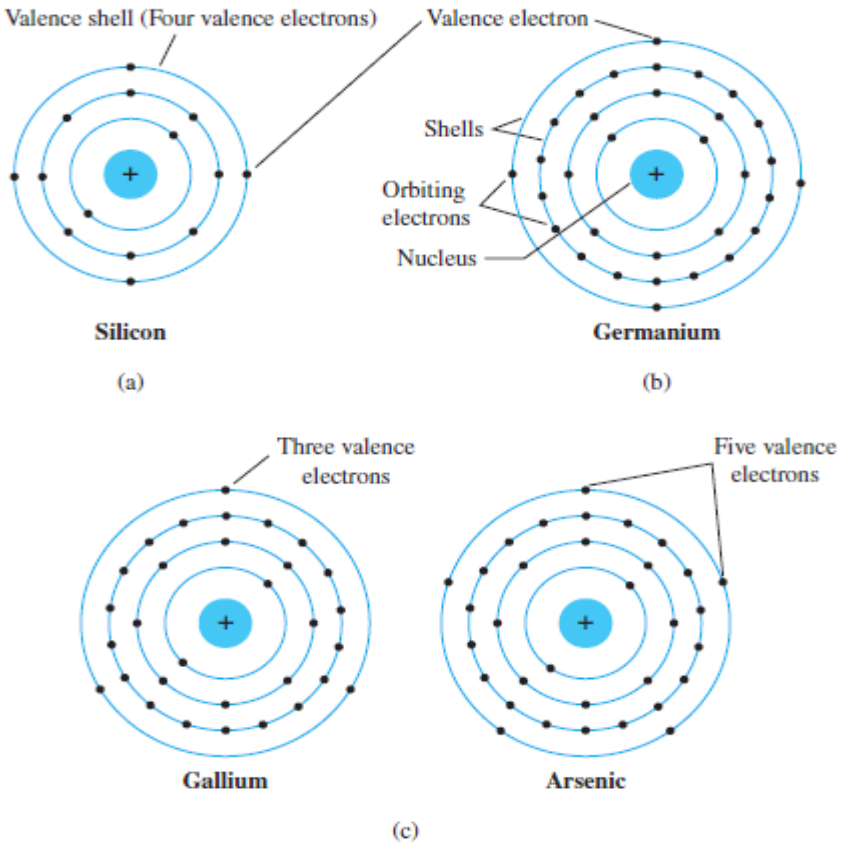


FIG. 1.3
Atomic structure of (a) silicon; (b) germanium; and (c) gallium and arsenic.

As indicated in Fig. 1.3 , silicon has 14 orbiting electrons, germanium has 32 electrons, gallium has 31 electrons, and arsenic has 33 orbiting electrons (the same arsenic that is a very poisonous chemical agent). For germanium and silicon there are four electrons in the outermost shell, which are referred to as valence electrons . Gallium has three valence electrons and arsenic has five valence electrons. Atoms that have four valence electrons are called **tetravalent**, those with three are called **trivalent**
, and those with five are called **pentavalent** . The term valence is used to indicate that the potential (ionization potential) required to remove any one of these electrons from the atomic structure is significantly lower than that required for any other electron in the structure.

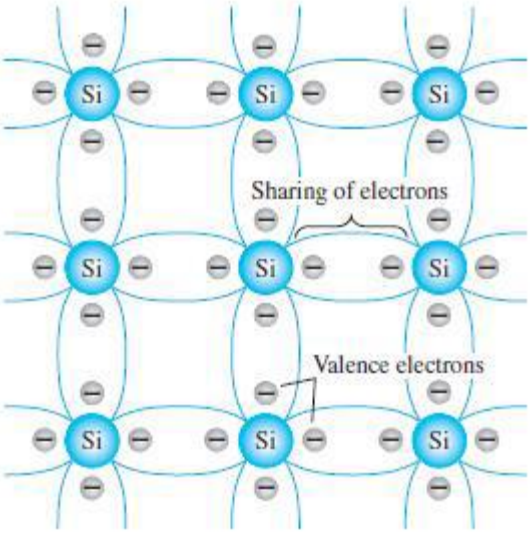


FIG. 1.4
Covalent bonding of the silicon atom.

This bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Although the covalent bond will result in a stronger bond between the valence electrons and their parent atom, it is still possible for the valence electrons to absorb sufficient kinetic energy from external natural causes to break the covalent bond and assume the "free" state.

The term *free* is applied to any electron that has separated from the fixed lattice structure and is very sensitive to any applied electric fields such as established by voltage sources or any difference in potential. ***The external causes include effects such as light energy in the form of photons and thermal energy (heat) from the surrounding medium***.

The term intrinsic is applied to any semiconductor material that has been carefully Refined to reduce the number of impurities to a very low level—essentially as pure as can be made available through modern technology.

.The free electrons in a material due only to external causes are referred to as ***intrinsic carriers*.**

Table 1.1 compares the number of intrinsic carriers per cubic centimeter (abbreviated n_i) for Ge, Si, and GaAs. It is interesting to note that Ge has the highest number and GaAs the lowest. In fact, Ge has more than twice the number as GaAs.

The number of carriers in the intrinsic form is important, but other characteristics of the material are more significant in determining its use in the field. One such factor is the *relative mobility* (μ_n) of the free carriers in the material, that is, the ability of the free carriers to move throughout the material.

Table 1.2 clearly reveals that the free carriers in GaAs have more than five times the mobility of free carriers in Si, a factor that results in response times using GaAs electronic devices that can be up to five times those of the same devices made from Si.

Note also that free carriers in Ge have more than twice the mobility of electrons in Si, a factor that results in the continued use of Ge in high-speed radio frequency applications

TABLE 1.1
Intrinsic Carriers n_i

Semiconductor	Intrinsic Carriers (per cubic centimeter)
GaAs	1.7×10^6
Si	1.5×10^{10}
Ge	2.5×10^{13}

TABLE 1.2
Relative Mobility Factor μ_n

Semiconductor	μ_n ($cm^2/V \cdot s$)
Si	1500
Ge	3900
GaAs	8500

1.4 ENERGY LEVELS

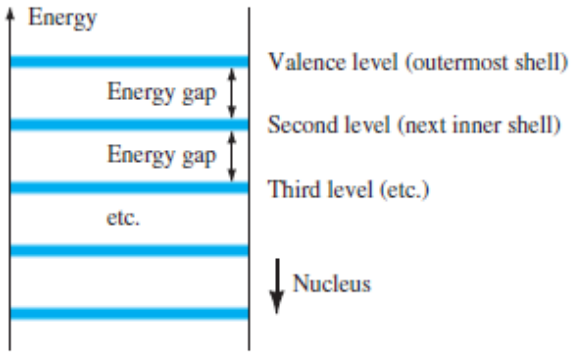
Within the atomic structure of each and every isolated atom there are specific energy levels associated with each shell and orbiting electron, as shown in Fig.1.6.

The energy levels associated with each shell will be different for every element. However, in general:

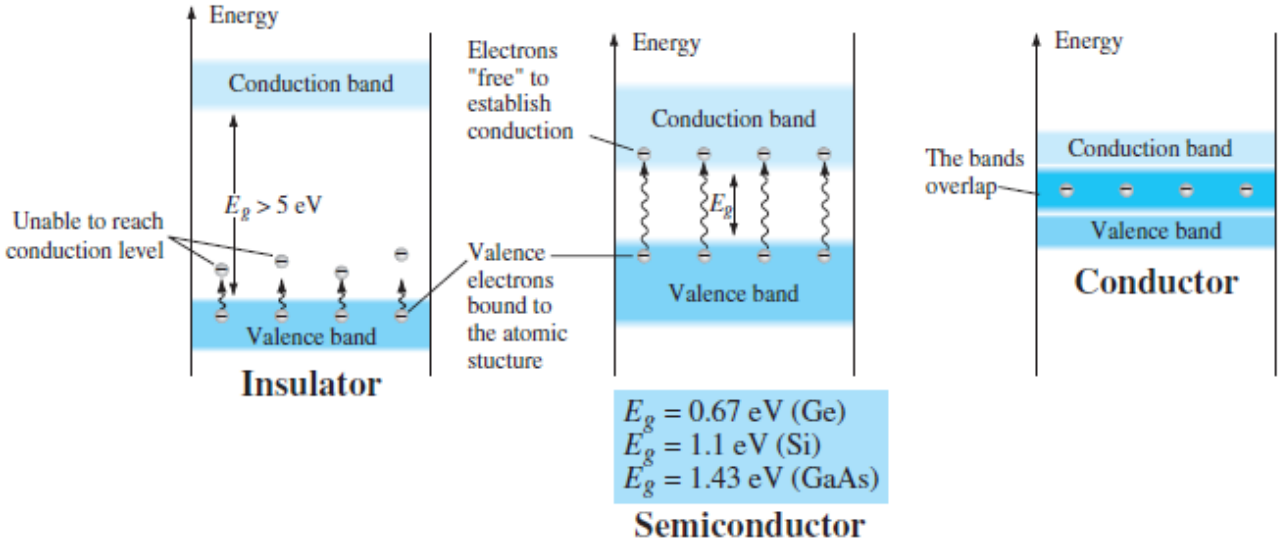
The farther an electron is from the nucleus, the higher is the energy state, and any electron that has left its parent atom has a higher energy state than any electron in the atomic structure.

Note in Fig. 1.6a that only specific energy levels can exist for the electrons in the atomic structure of an isolated atom. The result is a series of gaps between allowed energy levels

SEMICONDUCTOR DIODES



(a)



(b)

An electron in the valence band of silicon must absorb more energy than one in the valence band of germanium to become a free carrier. Similarly, an electron in the valence band of gallium arsenide must gain more energy than one in silicon or germanium to enter the conduction band.

الوحدة الأولى - المحاضرة الثانية - الزمن: 120 دقيقة

أهداف المحاضرة الثانية:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

التعرف على عدد من الدايودات المختلفة ومعرفة الفرق بينها

موضوعات المحاضرة الثانية:

n -TYPE AND p -TYPE MATERIALS

SEMICONDUCTOR DIODE

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة • سؤال وجواب	• جهاز حاسوب • جهاز عرض • سبورة • اوراق واقلام

المادة العلمية:

1.5 *n* -TYPE AND *p* -TYPE MATERIALS

A semiconductor material that has been subjected to the doping process is called an extrinsic material.

There are two extrinsic materials of immeasureable importance to semiconductor device fabrication: *n* -type and *p* -type materials. Each is described in some detail in the following subsections.

n -Type Material

An n -type material is created by introducing impurity elements that have five valence electrons(pentavalent), such as antimony , arsenic , and phosphorus The effect of such impurity elements is indicated inFig. 1.7 (using antimony as the impurity in a silicon base). Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is unassociated with any particular covalent bond, This remaining electron, loosely تامه حريه في bound to its parent (antimony) atom,

المنتشره الشوائب Diffused impurities with five valence electrons are called donor المانحه atoms.

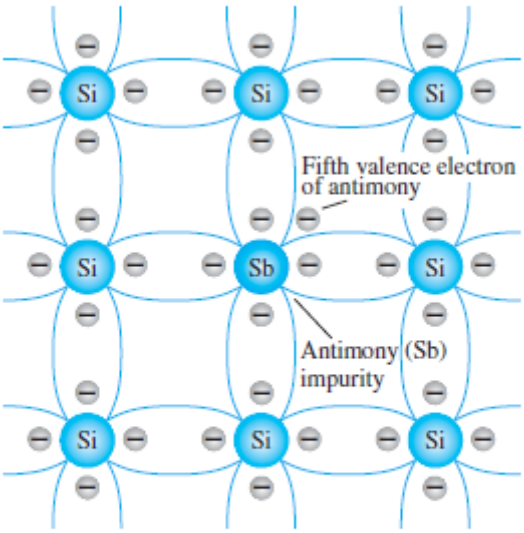


FIG. 1.7
Antimony impurity in n-type material.

The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.8 . Note that a discrete energy level (called the *donor level*) appears in the forbidden band with an *Eg* significantly less than that of the intrinsic material.

Those free electrons due to the added impurity sit at this energy level and have less difficulty absorbing a sufficient measure of thermal energy to move into the conduction band at room temperature.

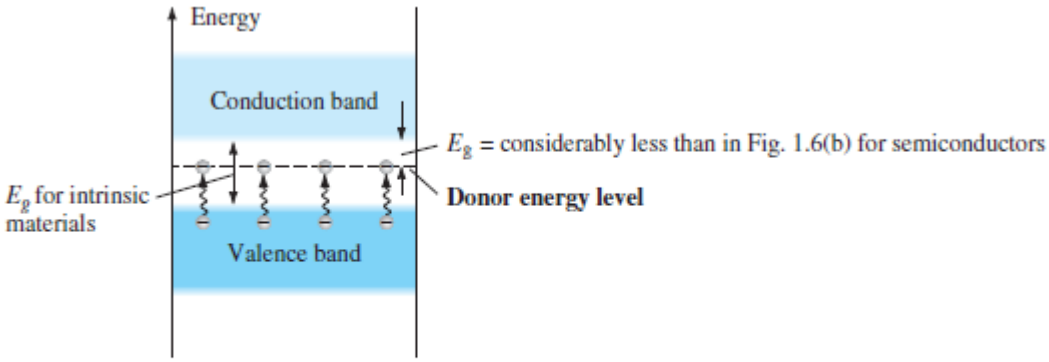


FIG. 1.8
Effect of donor impurities on the energy band structure.

p -Type Material

The p -type material is formed by doping a pure germanium or silicon crystal with impurity atoms having three valence electrons. The elements most frequently used for this purpose are boron , gallium , and indium . Each is a member of a subset group of elements in the Periodic Table of Elements referred to as Group III because each has three valence electrons. The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.9 .

Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a hole and is represented by a small circle or a plus sign, indicating the absence of a negative charge. Since the resulting vacancy will readily accept a free electron:

The diffused impurities with three valence electrons are called acceptor atoms.

The resulting p -type material is electrically neutralمحايد , for the same reasons described for the n -type material.

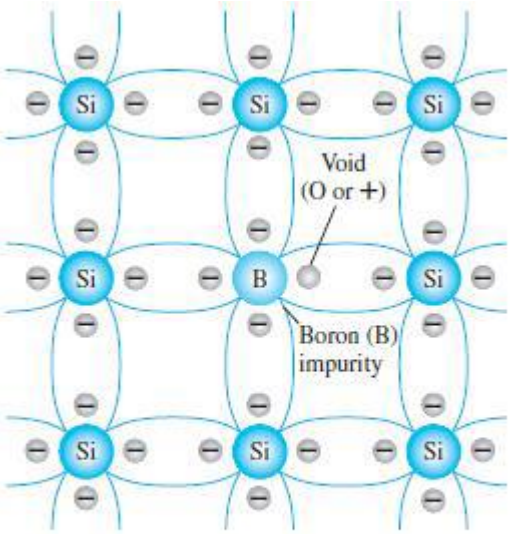


FIG. 1.9
Boron impurity in p-type material.

Electron versus Hole Flow

The effect of the hole on conduction is shown in Fig. 1.10 . If a valence electron acquires sufficient kinetic energy to break its covalent bond and fills the void created by a hole, then a vacancy, or hole, will be created in the covalent bond that released the electron. There is, therefore, a transfer of holes to the left and electrons to the right, as shown in Fig. 1.10 .

The direction to be used in this text is that of *conventional flow* , which is indicated by the direction of hole flow.

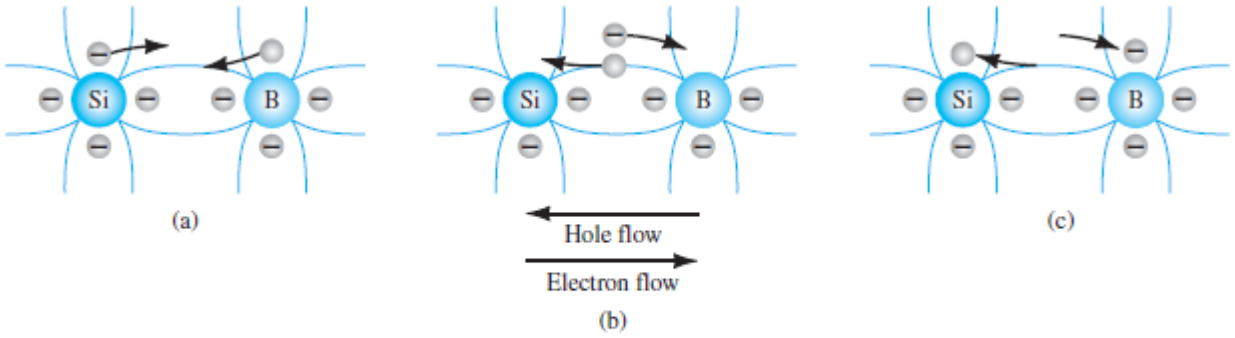
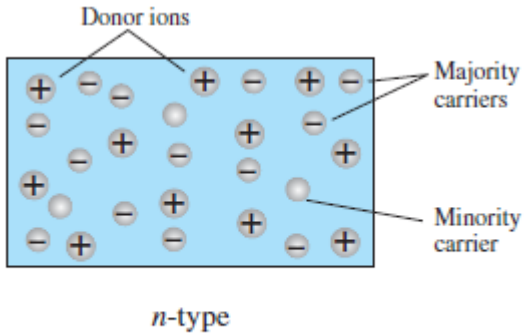


FIG. 1.10
Electron versus hole flow.

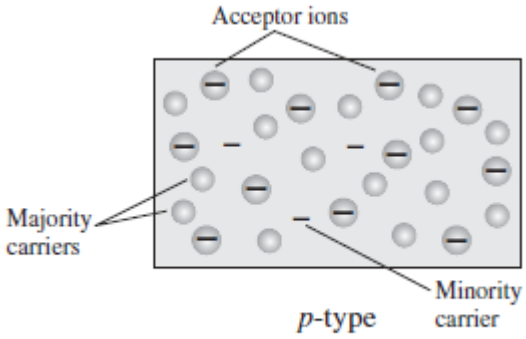
Majority and Minority Carriers

In an n-type material (Fig. 1.11a) the electron is called the majority carrier and the hole the minority carrier.



(a)

In a p-type material the hole is the majority carrier and the electron is the minority carrier. For the p -type material the number of holes far outweighs تفوق the number of electrons,



(b)

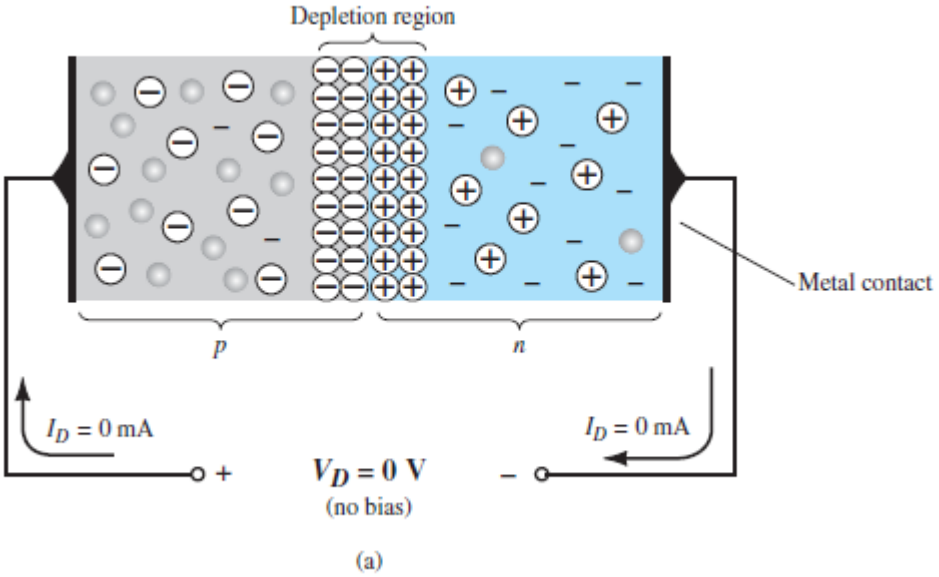
1.6 SEMICONDUCTOR DIODE

Now that both n - and p -type materials are available, we can construct our first solid-state electronic device: The semiconductor diode, is created by simply joining an *n* -type and a *p* -type material together

No Applied Bias (V_0 V)

At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack قليل of free carriers in the region near the junction, as shown in Fig. 1.12a . Note in Fig. 1.12a that the only particles displayed in this region are the positive and the negative ions remaining once the free carriers have been absorbed.

This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.



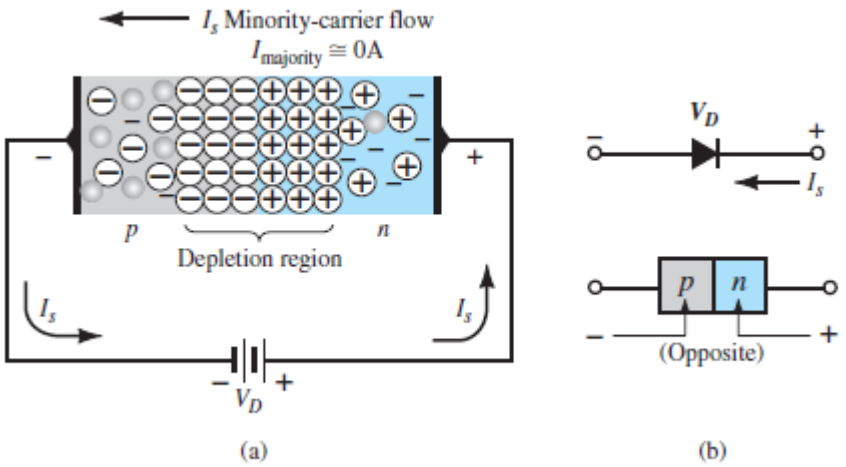
Under no-bias conditions, any minority carriers (holes) in the *n* -type material that find themselves within the depletion region for any reason whatsoever ايا كان will pass quickly into the *p* -type material. The closer the minority carrier is to the junction, the greater is the attraction جاذبيه for the layer of negative ions and the less is the opposition offered by the positive ions in the depletion region of the *n* -type material. We will conclude, therefore, for future discussions, that any minority carriers of the *n* -type material that find themselves in the depletion region will pass directly into the *p* -type material. This carrier flow is indicated at the top of Fig. 1.12c for the minority carriers of each material.

In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.

Reverse-Bias Condition (*V D* > 0 V)

If an external potential of *V* volts is applied across the *p* – *n* junction such that the positive terminal is connected to the *n* -type material and the negative terminal is connected to the *p* -type material as shown in Fig. 1.13 , the number of uncovered positive ions in the depletion region of the *n* -type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p* -type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero, as shown in Fig. 1.13a

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by Is .



Forward-Bias Condition (V D + 0 V)

A forward-bias or "on" condition is established by applying the positive potential to the p -type material and the negative potential to the n -type material as shown in Fig. 1.14 . The application of a forward-bias potential V D will "pressure" electrons in the n -type material and holes in the p -type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.14a . The resulting minority-carrier flow of electrons from the *p* -type material to the *n* -type material (and of holes from the *n* -type material to the *p* -type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction

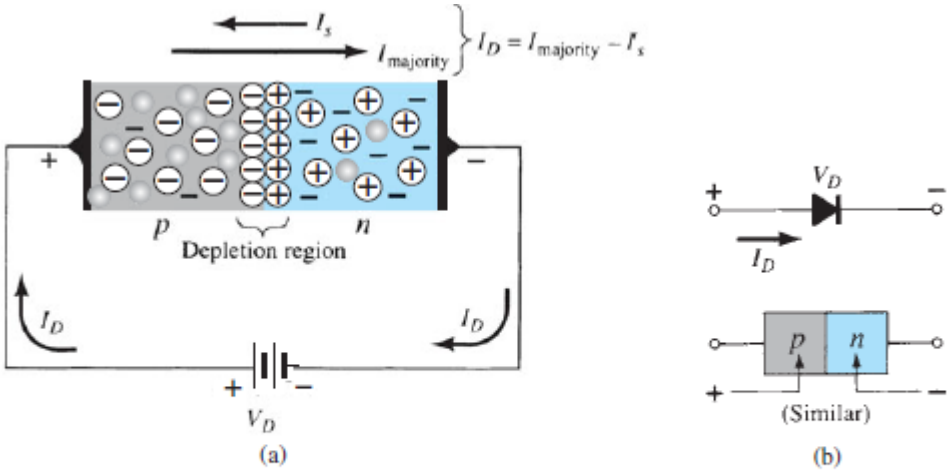


FIG. 1.14

Forward-biased p–n junction: (a) internal distribution of charge under forward-bias conditions; (b) forward-bias polarity and direction of resulting current.

Breakdown Region

The reverse-bias potential that results in this dramatic change in characteristics is called the breakdown potential and is given the label VBV .

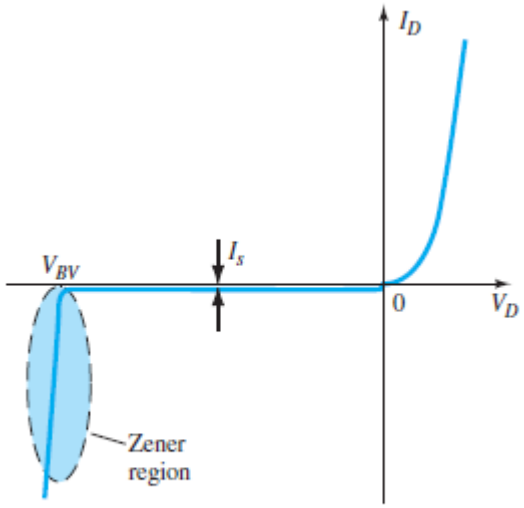


FIG. 1.17
Breakdown region.

The maximum reverse-bias potential that can be applied before entering the breakdown region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted the PRV rating).

الوحدة الثانية - المحاضرة الثالثة - الزمن: 120 دقيقة

أهداف المحاضرة:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

1. Understand the concept of load-line analysis and how it is applied to diode networks.
2. Become familiar with the use of equivalent circuits to analyze series, parallel, and series-parallel diode networks.
3. Understand the process of rectification to establish a dc level from a sinusoidal ac input.

موضوعات المحاضرة الثانية:

DC diode applications

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة سؤال وجواب	• جهاز حاسوب • جهاز عرض • سبورة اوراق واقلام

المادة العلمية:

LOAD-LINE ANALYSIS

The circuit of Fig. 2.1 is the simplest of diode configurations. It will be used to describe the analysis of a diode circuit using its actual characteristics. In the next section we will replace the characteristics by an approximate model for the diode and compare solutions. Solving the circuit of Fig. 2.1 is all about finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

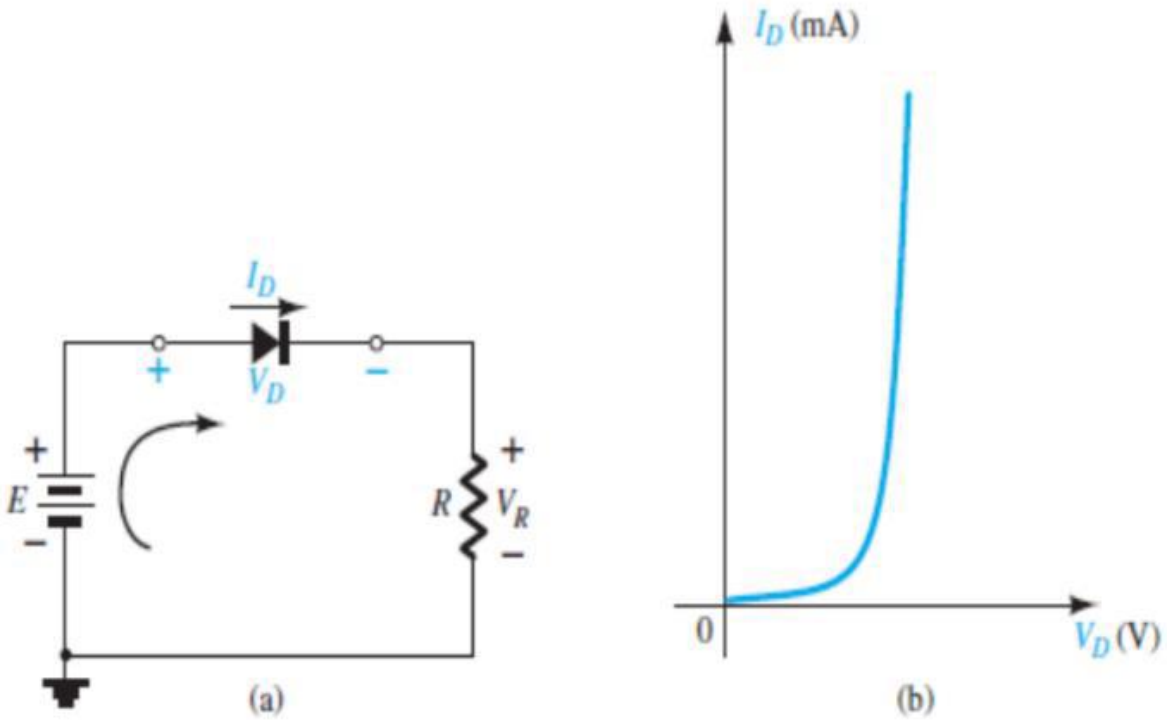


FIG. 2.1
Series diode configuration: (a) circuit; (b) characteristics.

In Fig. 2.2 the diode characteristics are placed on the same set of axes as a straight line defined by the parameters of the network. The straight line is called a load line because the intersection on the vertical axis is defined by the applied load R . The analysis to follow is therefore called load-line analysis. The intersection of the two curves will define the solution for the network and define the current and voltage

$$+E - V_D - V_R = 0$$

$$V_D = E|_{I_D=0\,\text{A}}$$

$$E = V_D + I_D R$$

$$I_D = \frac{E}{R}\bigg|_{V_D=0\,\text{V}}$$

load line

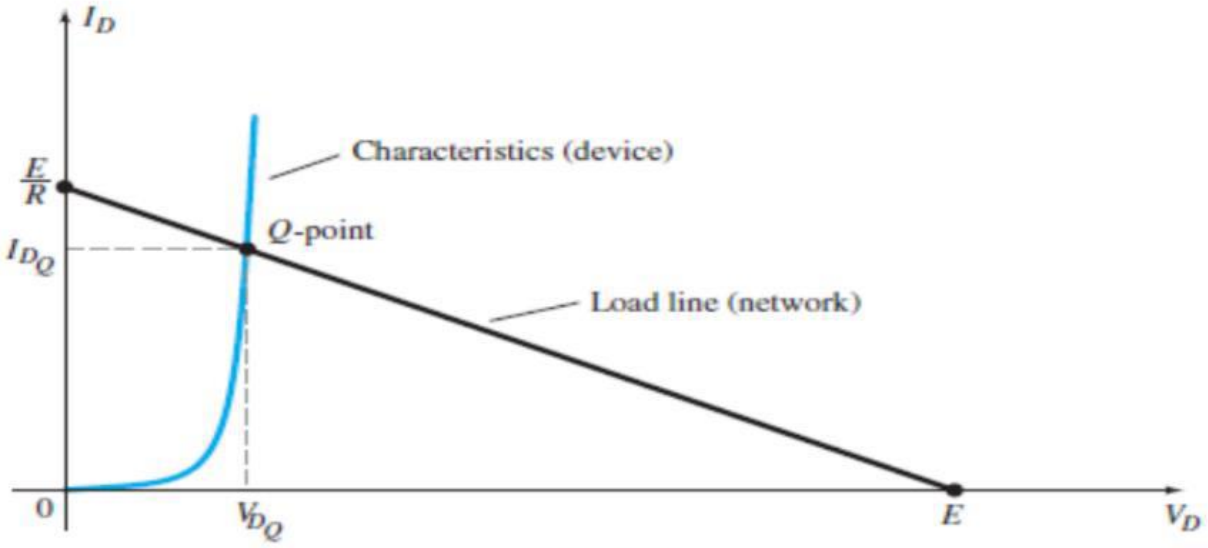
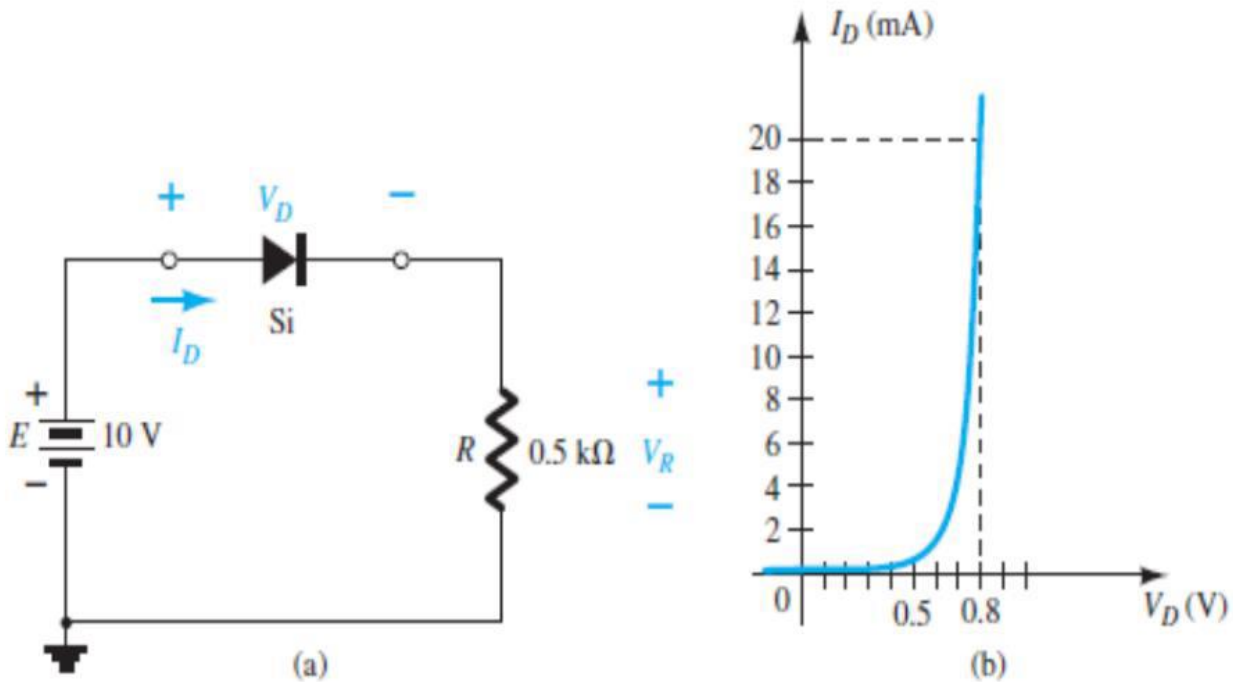


FIG. 2.2
Drawing the load line and finding the point of operation.

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a , employing the diode characteristics of Fig. 2.3b , determine: a. V_{DQ} and I_{DQ}. b. V_R .



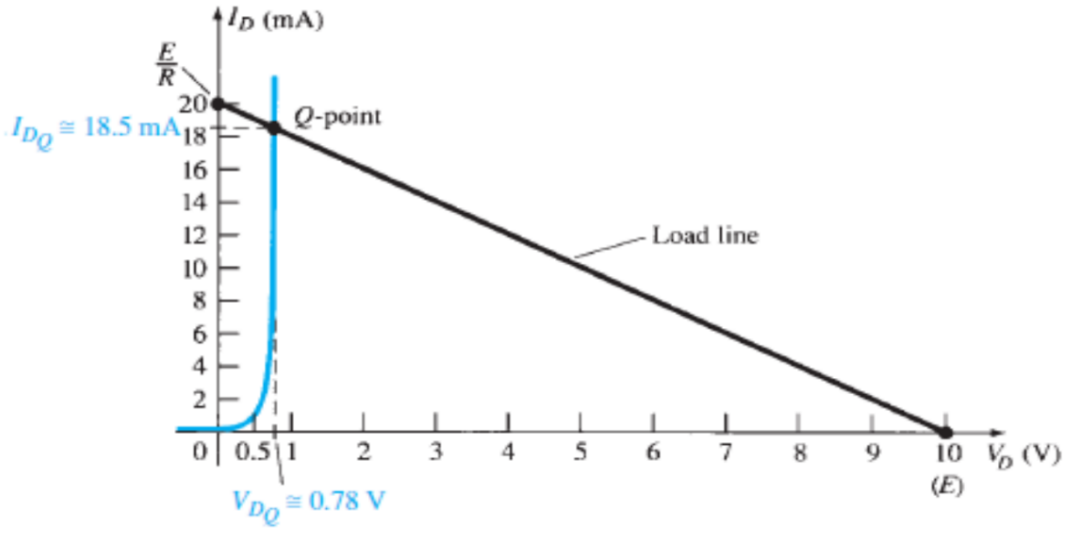


FIG. 2.4
Solution to Example 2.1.

Using the *Q*-point values, the dc resistance for Example 2.1 is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.78\text{ V}}{18.5\text{ mA}} = 42.16\ \Omega$$

An equivalent network (for these operating conditions only) can then be drawn as shown in Fig. 2.5.

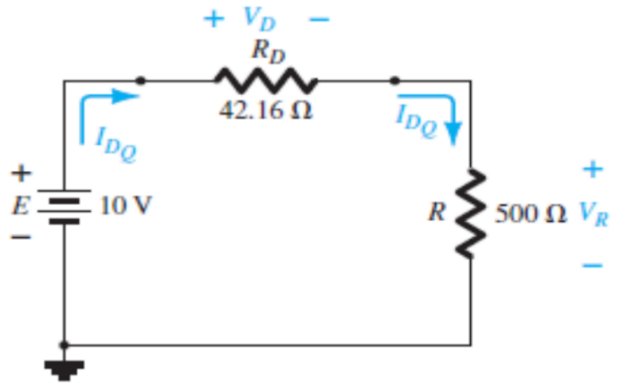


FIG. 2.5
Network quivalent to Fig. 2.4.

The current

$$I_D = \frac{E}{R_D + R} = \frac{10\text{ V}}{42.16\ \Omega + 500\ \Omega} = \frac{10\text{ V}}{542.16\ \Omega} \cong \mathbf{18.5\text{ mA}}$$

and

$$V_R = \frac{RE}{R_D + R} = \frac{(500\ \Omega)(10\text{ V})}{42.16\ \Omega + 500\ \Omega} = \mathbf{9.22\text{ V}}$$

SERIES DIODE CONFIGURATIONS

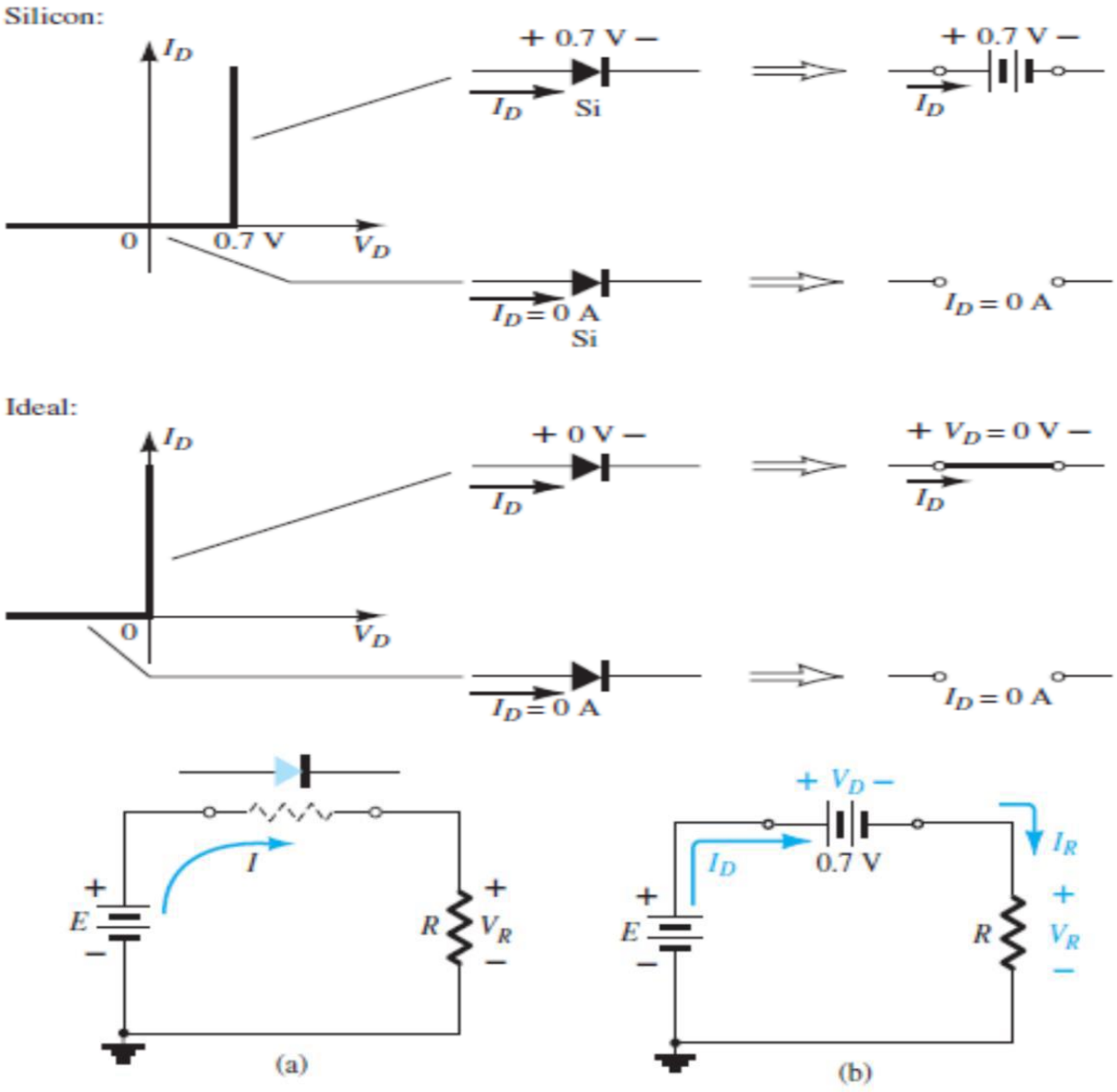


FIG. 2.9

(a) Determining the state of the diode of Fig. 2.8; (b) substituting the equivalent model for the "on" diode of Fig. 2.9a.

In Fig. 2.10 the diode of Fig. 2.7 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.11 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.12 . Due to the open circuit, the diode current is 0 A and the
voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = 0\text{ V}$$

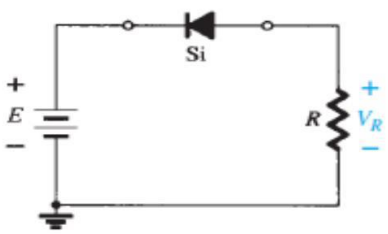


FIG. 2.10
Reversing the diode of Fig. 2.8.

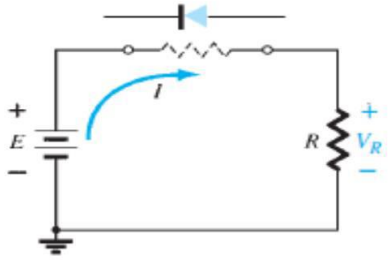


FIG. 2.11
Determining the state of the diode of Fig. 2.10.

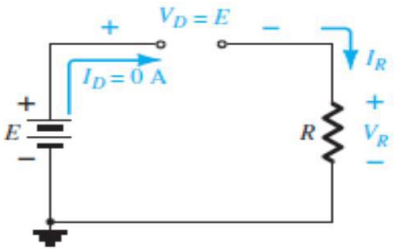


FIG. 2.12
Substituting the equivalent model for the "off" diode of Fig. 2.10.

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13 , determine V_D , V_R , and I_D

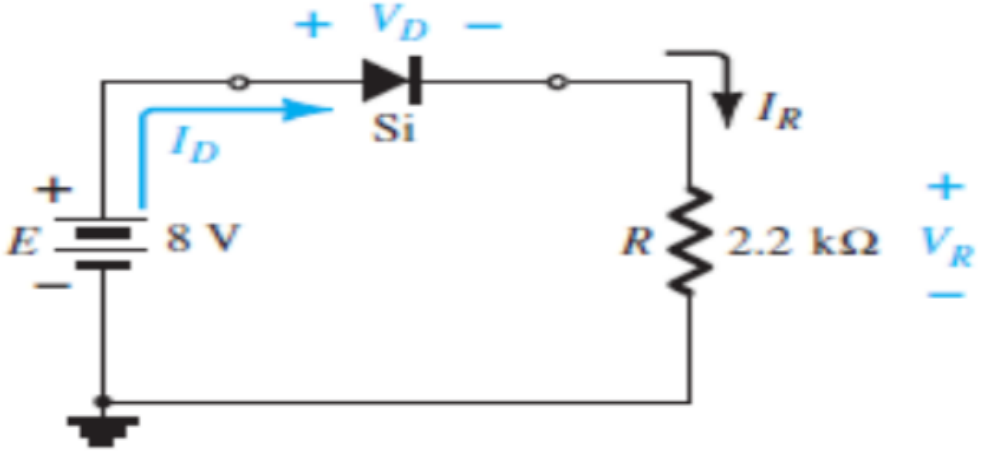


FIG. 2.13
Circuit for Example 2.4.

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = 0.7\text{ V}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = 7.3\text{ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong 3.32\text{ mA}$$

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16 , determine V_D , V_R , and I_D

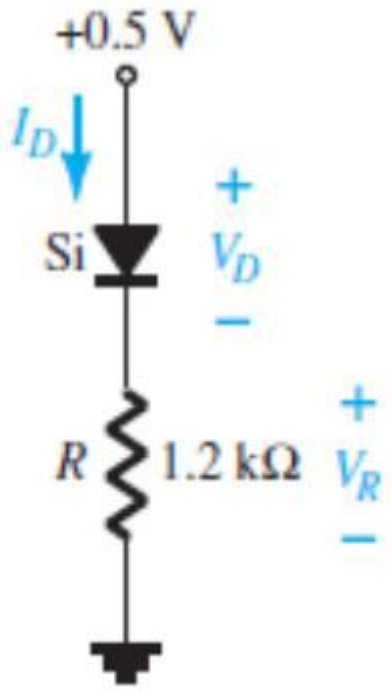


FIG. 2.16
Series diode circuit for Example 2.6.

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

$$I_D = 0\ \text{A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})\,1.2\ \text{k}\Omega = 0\ \text{V}$$

and

$$V_D = E = 0.5\ \text{V}$$

EXAMPLE 2.8 Determine I_D, V_{D2}, and Vo for the circuit of Fig. 2.21 ..
Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22 . There is a match in current direction for one silicon diode but not for the other silicon diode. The combination of a short circuit in series with an open circuit always results in an open circuit and I D 0 A, as shown in Fig. 2.23 .

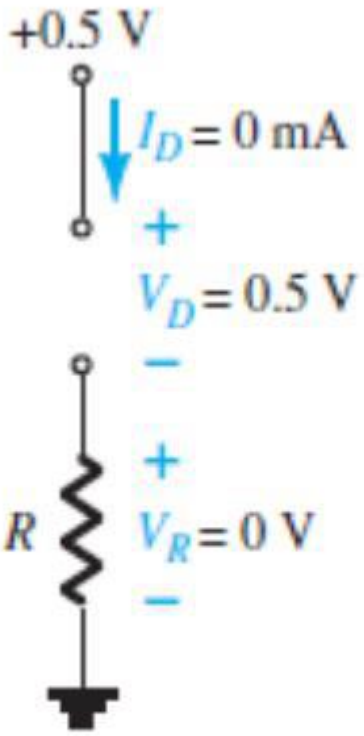


FIG. 2.18
Determining I_D, V_R, and V_D for the circuit of Fig. 2.16.

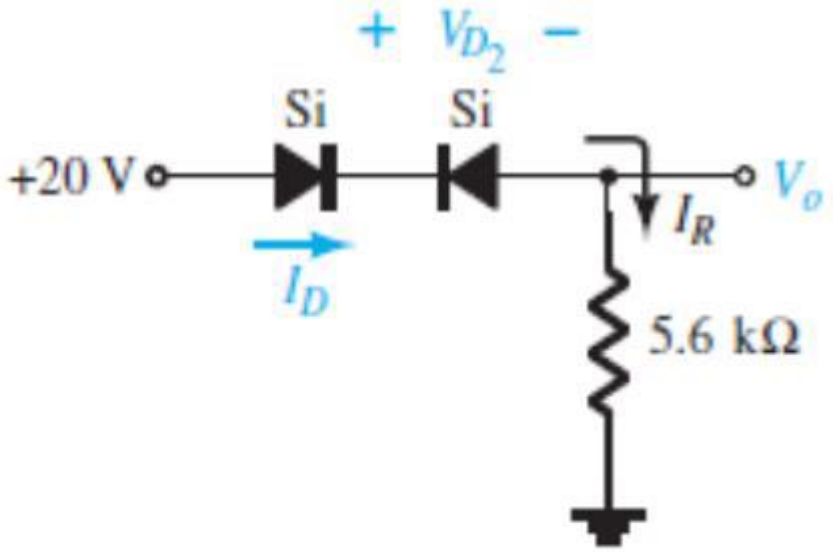


FIG. 2.21
Circuit for Example 2.8.

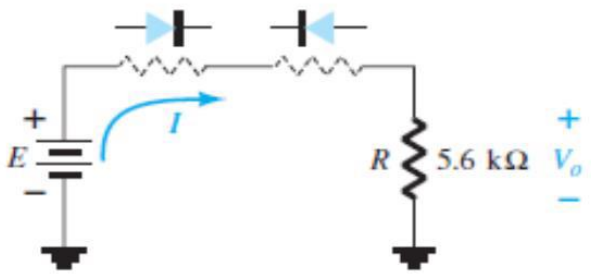


FIG. 2.22
Determining the state of the diodes of Fig. 2.21.

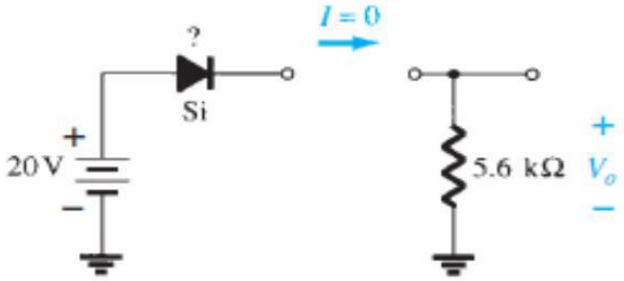


FIG. 2.23
Substituting the equivalent state for the open diode.

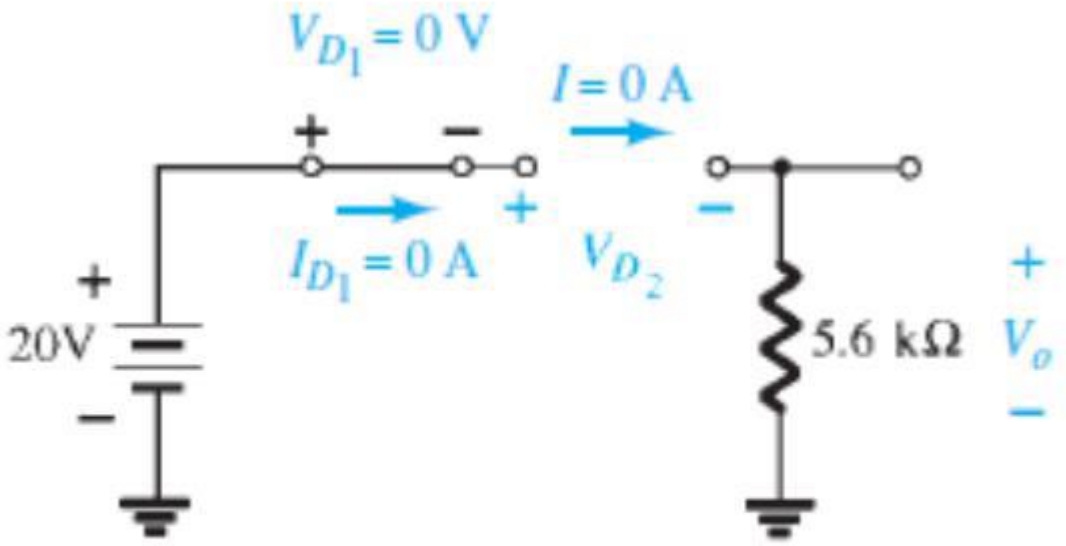


FIG. 2.24

Determining the unknown quantities for the circuit of Example 2.8.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.24. We have

$$V_o = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

and

$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{20\text{ V}}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and

$$V_{D_2} = E - V_{D_1} - V_o = 20\text{ V} - 0 - 0 = \mathbf{20\text{ V}}$$

with

$$V_o = \mathbf{0\text{ V}}$$

PARALLEL AND SERIES–PARALLEL CONFIGURATION

The methods applied in Section 2.3 can be extended to the analysis of parallel and series– parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.10 Determine Vo , I1 , ID1, and ID2 for the parallel diode configuration of Fig. 2.28

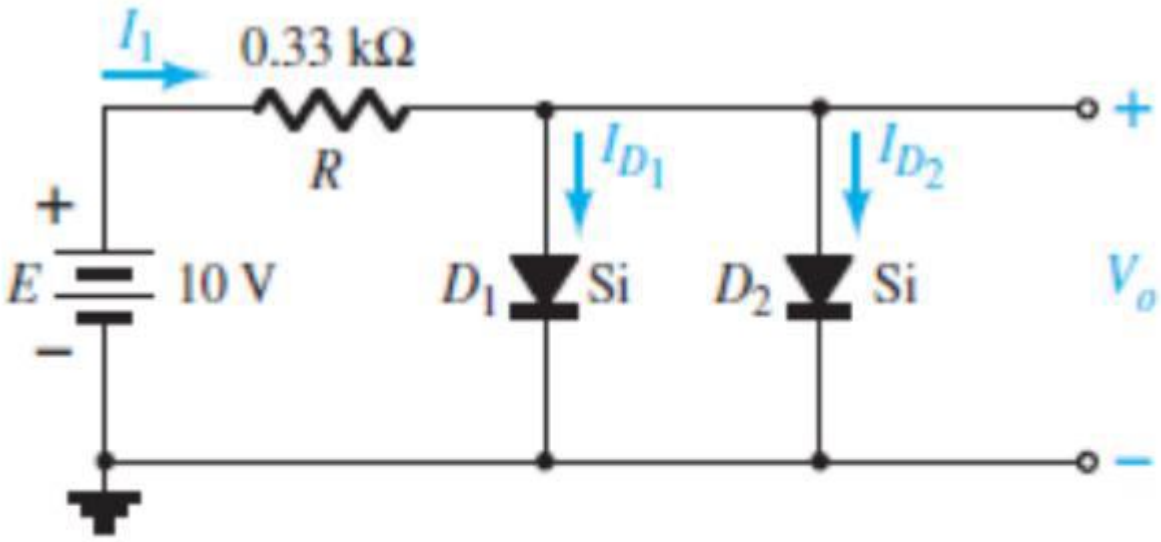


FIG. 2.28
Network for Example 2.10.

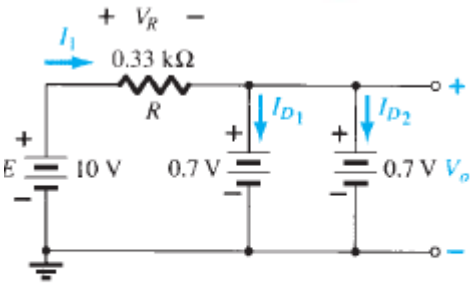


FIG. 2.29
Determining the unknown quantities for the network of Example 2.10.

Solution: For the applied voltage the "pressure" of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29 . Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always

the same and

$$V_o = 0.7\ \text{V}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\ \text{V} - 0.7\ \text{V}}{0.33\ \text{k}\Omega} = 28.18\ \text{mA}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\ \text{mA}}{2} = 14.09\ \text{mA}$$

EXAMPLE 2.13 Determine the currents I1 , I2 , and ID2 for the network of Fig. 2.37

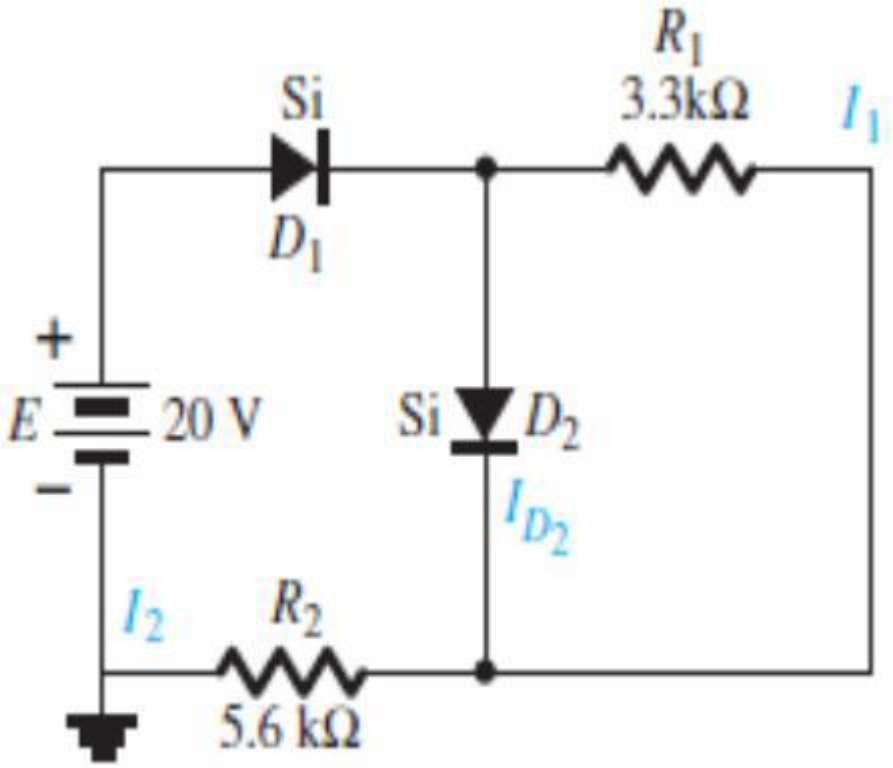


FIG. 2.37
Network for Example 2.13.

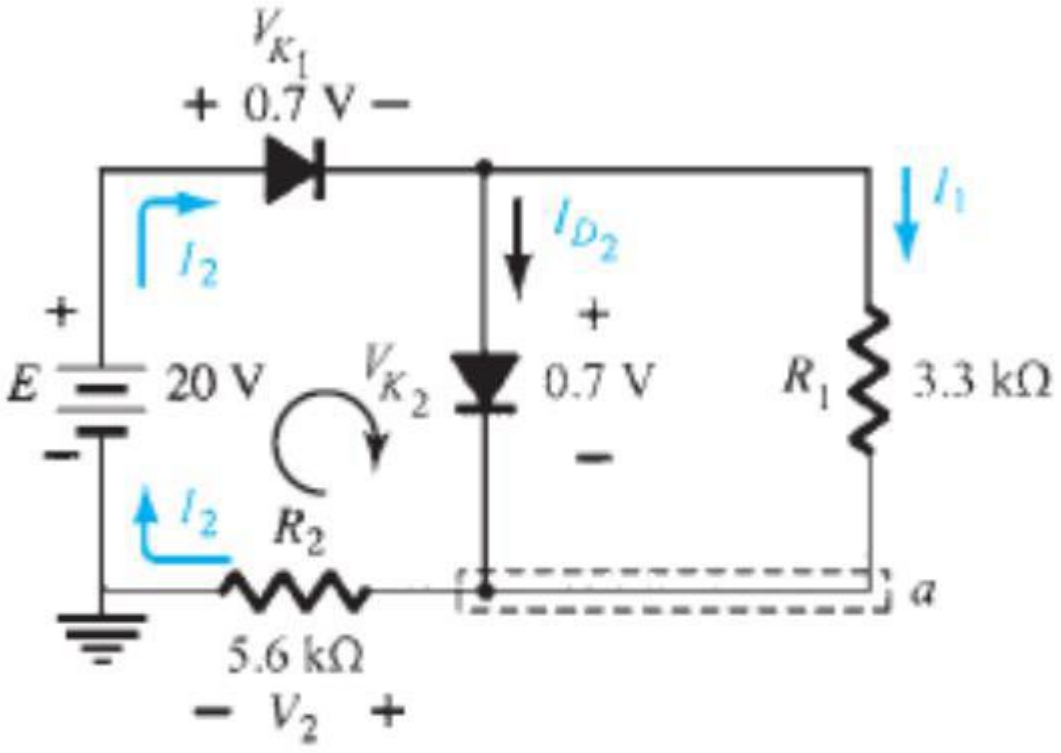


FIG. 2.38
Determining the unknown quantities for Example 2.13.

Solution: The applied voltage (pressure) is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38 . Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series–parallel networks. We have

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and

$$V_2 = E - V_{K_1} - V_{K_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{18.6\text{ V}}$$

with

$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node *a*,

$$I_{D_2} + I_1 = I_2$$

and

$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} \cong \mathbf{3.11\text{ mA}}$$

SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.44 . For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.

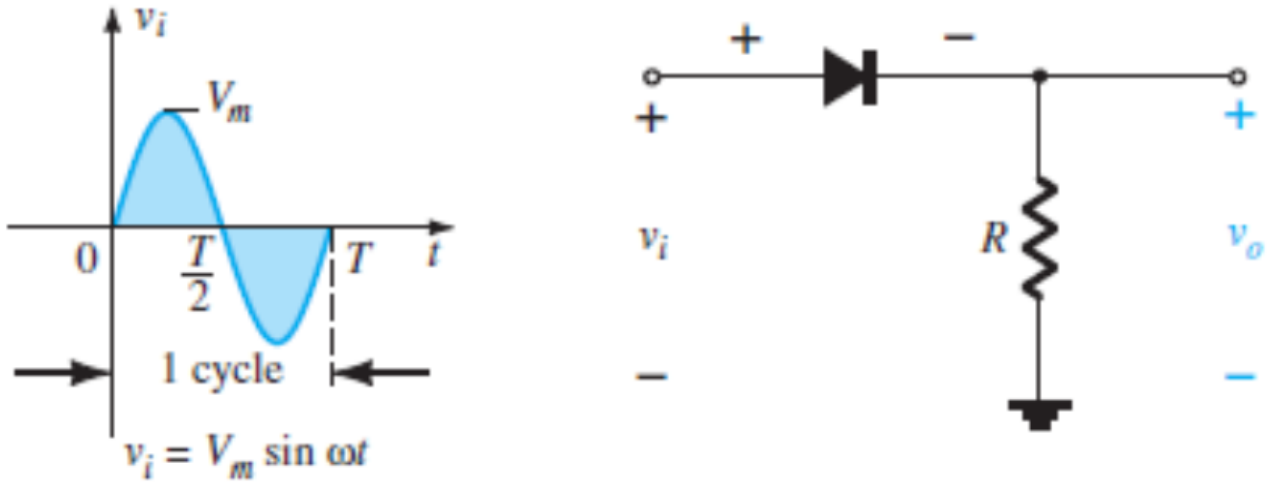


FIG. 2.44
Half-wave rectifier.

During the interval t = 0ST>2 in Fig. 2.44 the polarity of the applied voltage v i is such as to establish “pressure” in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.45 , where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode. For the period T>2ST, the polarity of the input v i is as shown in Fig. 2.46 , and the resulting polarity across the ideal diode produces an “off” state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and vo = iR = (0)R = 0 V for the period T>2ST. The input v i and the output v o are sketched together in Fig. 2.47 for comparison purposes. The output signal v o now has a net positive area above the axis over

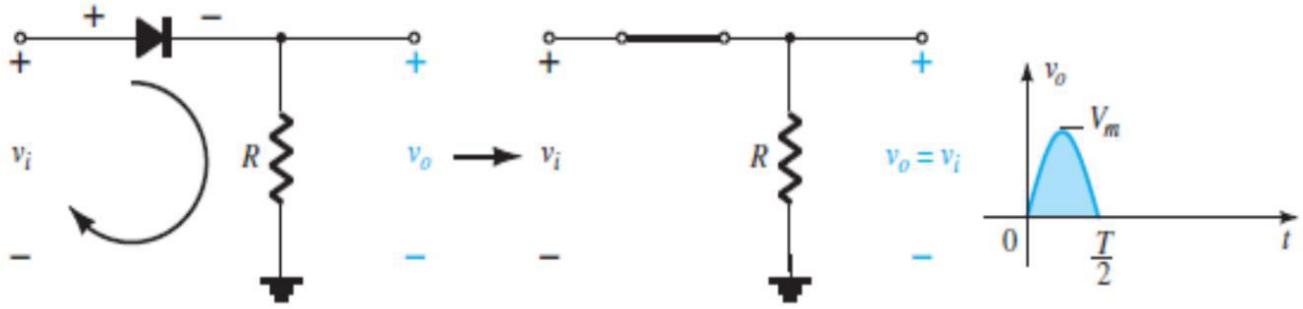


FIG. 2.45
Conduction region ($0 \rightarrow T/2$).

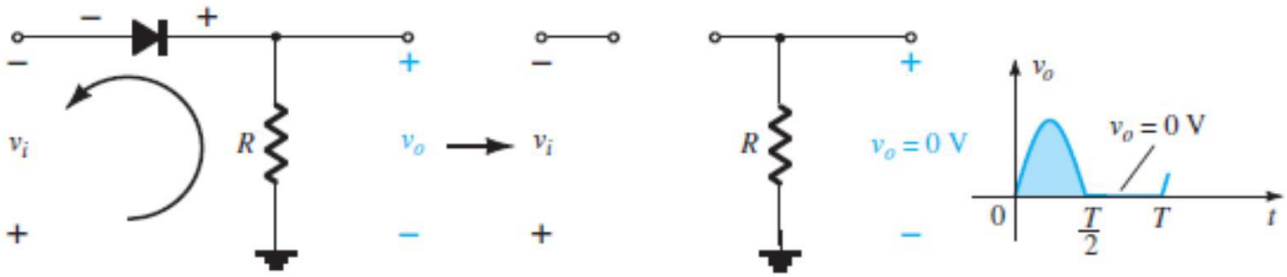
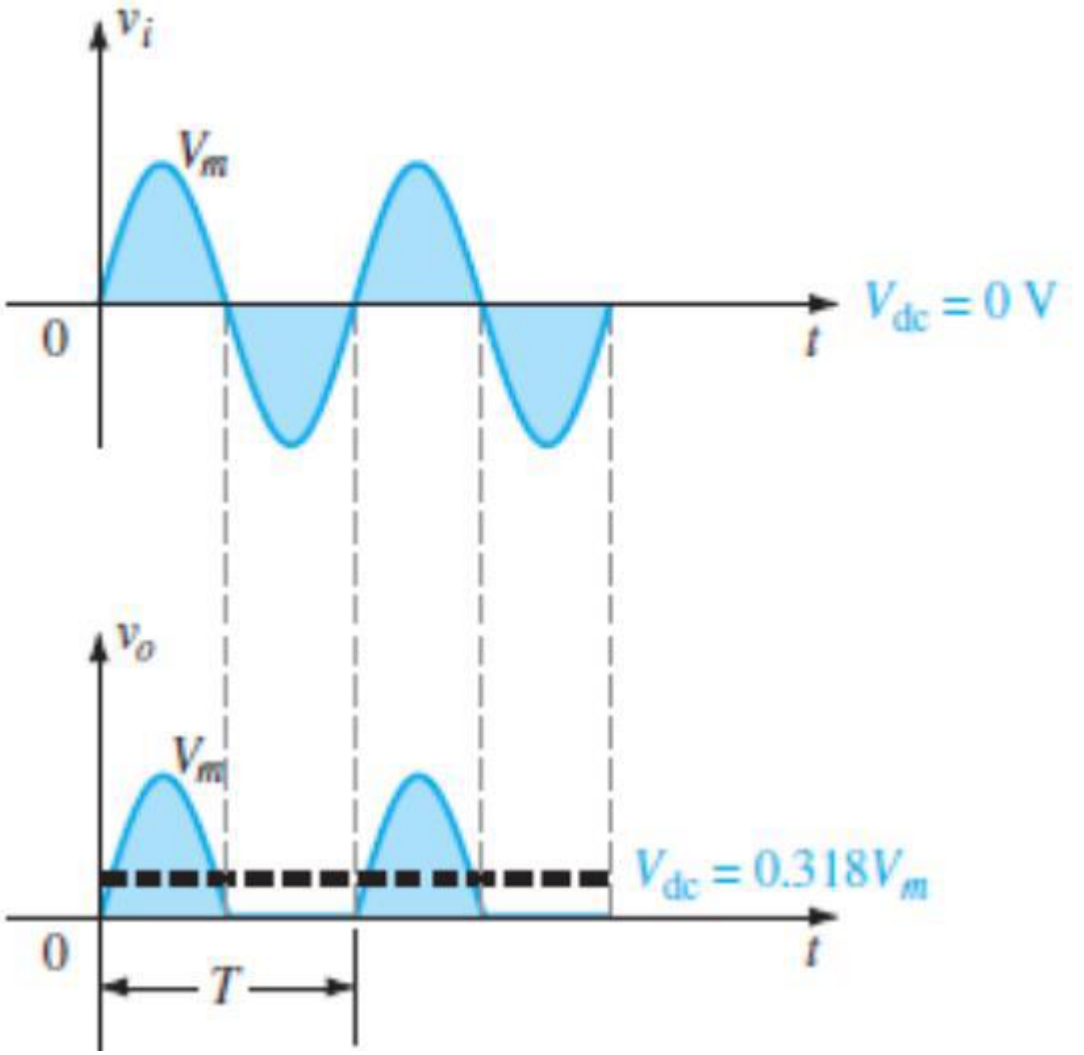


FIG. 2.46
Nonconduction region ($T/2 \rightarrow T$).



a full period and an average value determined by

$$V_{dc} = 0.318\,V_m$$ half-wave

The process of removing one-half the input signal to establish a dc level is called **half wave rectification**

The effect of using a silicon diode with V K 0.7 V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v i less than 0.7 V, the diode is still in an open- circuit state and v o 0 V, as shown in the same figure. When conducting, the difference between v o and v i is a fixed

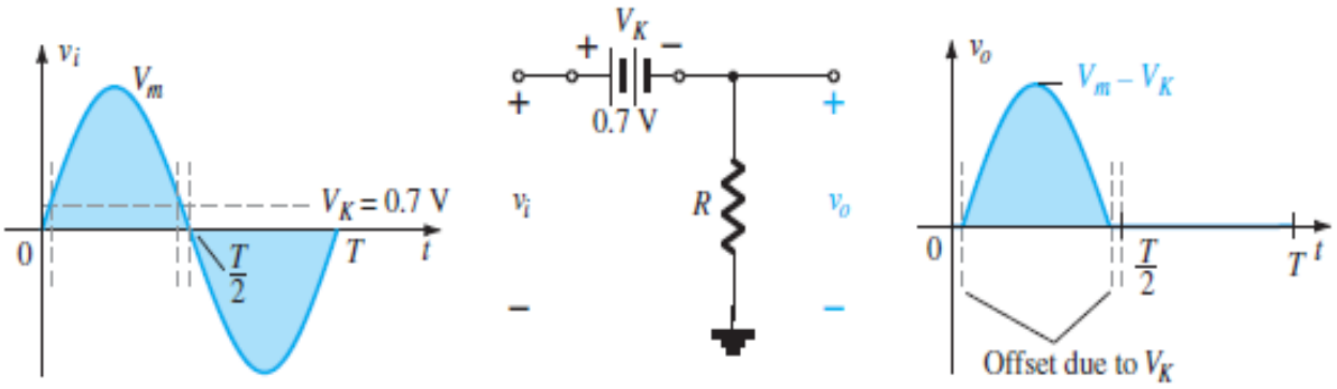


FIG. 2.48
Effect of V_K on half-wave rectified signal.

level of V K = 0.7 V and vo = vi - VK, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where Vm << VK, the following equation can be applied to determine the average value with a
relatively high level of accuracy

$$V_{dc} \cong 0.318(V_m - V_K)$$

EXAMPLE 2.16

a. Sketch the output v o and determine the dc level of the output for the network of Fig. 2.49

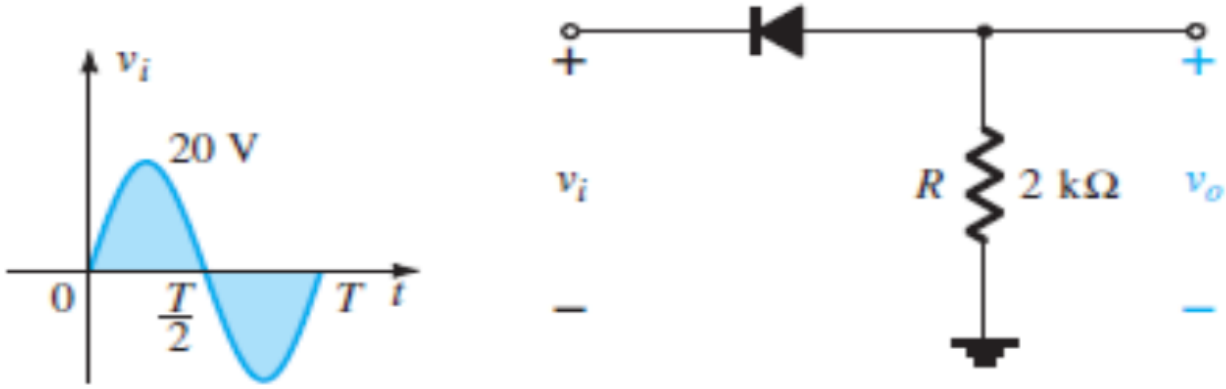


FIG. 2.49
Network for Example 2.16.

b.

Solution:
a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50 , and v o will appear as shown in the same figure. For the full period, the dc level is

Vdc = - 0.318 Vm = -0.318(20 V) = - 6.36 V
The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49 .

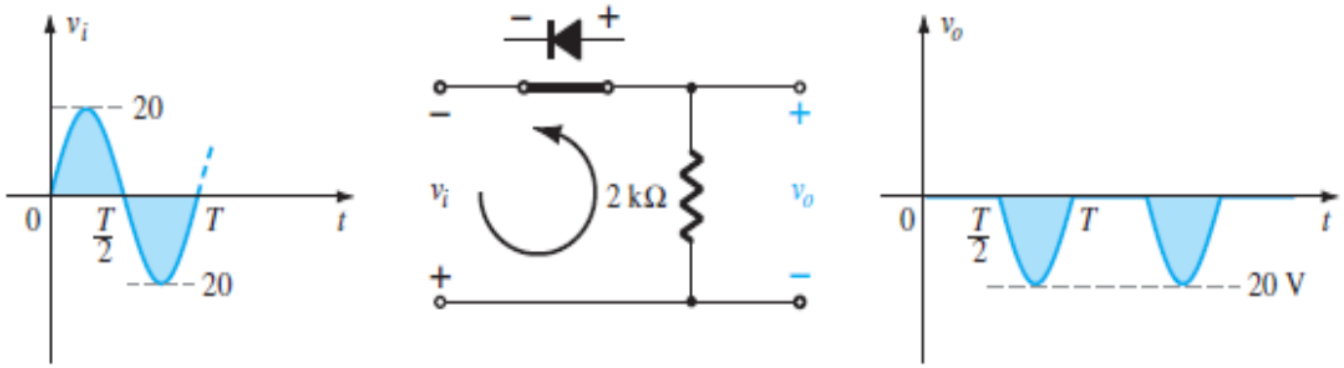


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

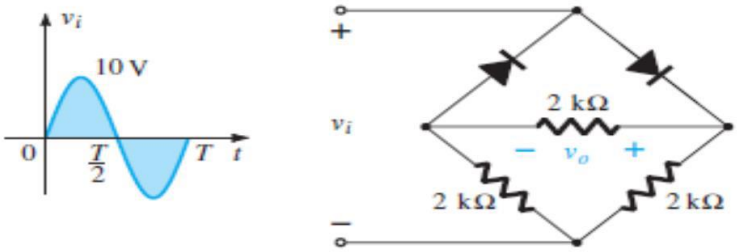
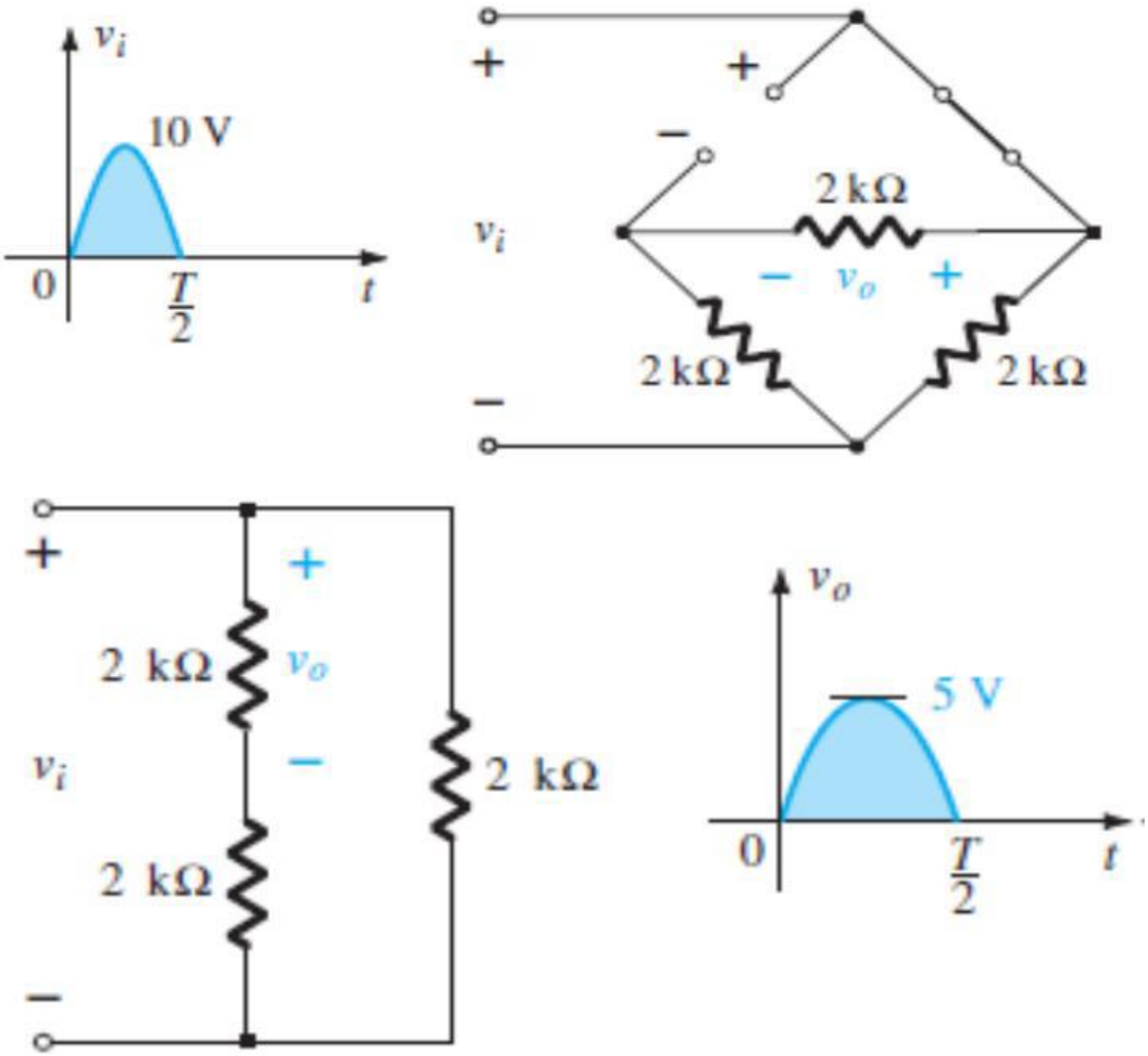


FIG. 2.64
Bridge network for Example 2.17.

$$V_{dc} = 0.636(5\text{ V}) = 3.18\text{ V}$$



Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v i applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. D 1 assumes the short-circuit equivalent and D 2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61

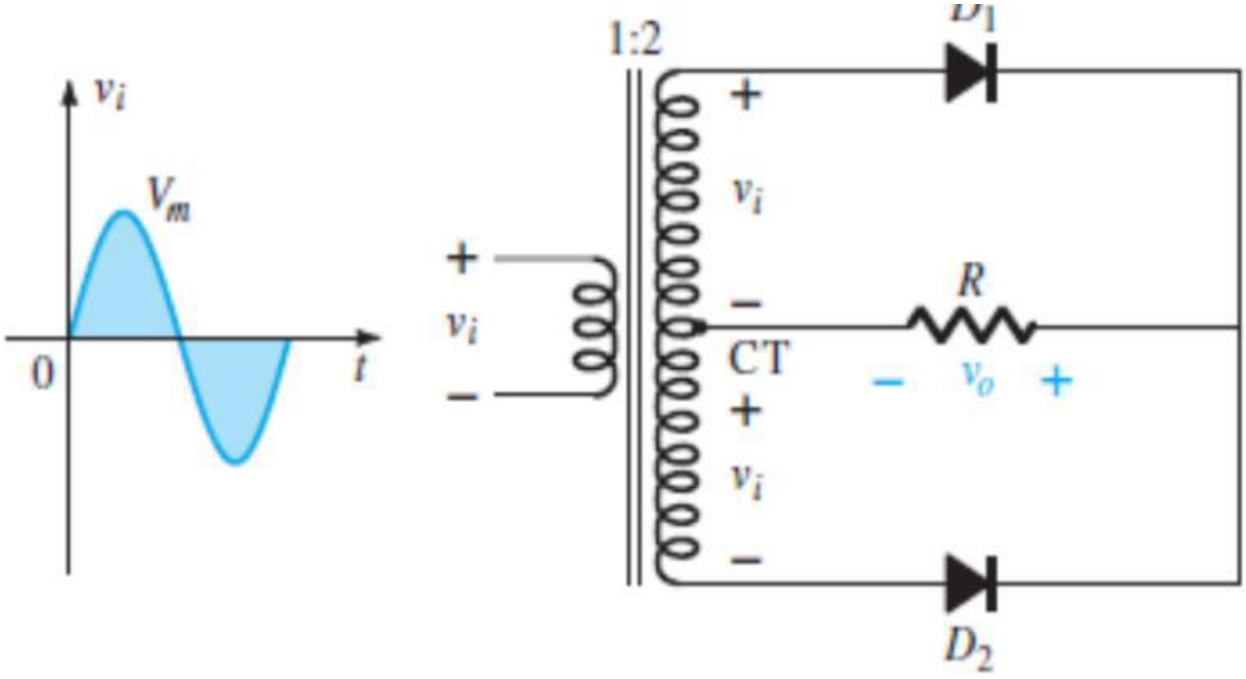
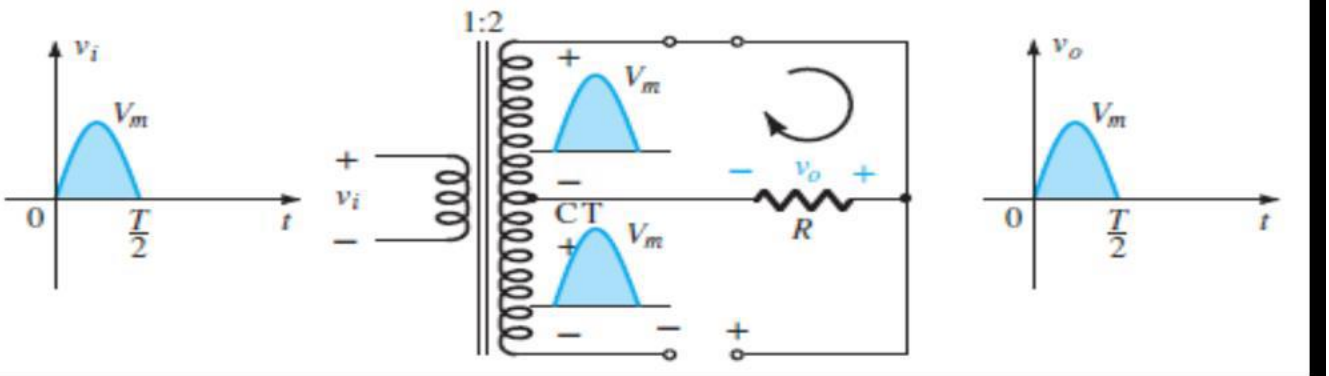


FIG. 2.60

Center-tapped transformer full-wave rectifier.



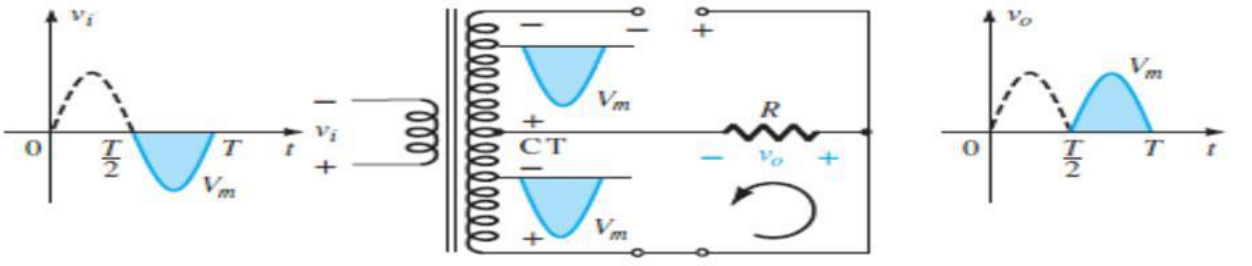


FIG. 2.62

Network conditions for the negative region of v_i.

الوحدة الثانية - المحاضرة الرابعة - الزمن: 120 دقيقة

موضوعات المحاضرة الثانية:

AC diode applications

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة سؤال وجواب اختبار	• جهاز حاسوب • جهاز عرض • سبورة اوراق واقلام

المادة العلمية:

2.8 CLIPPERS

Series

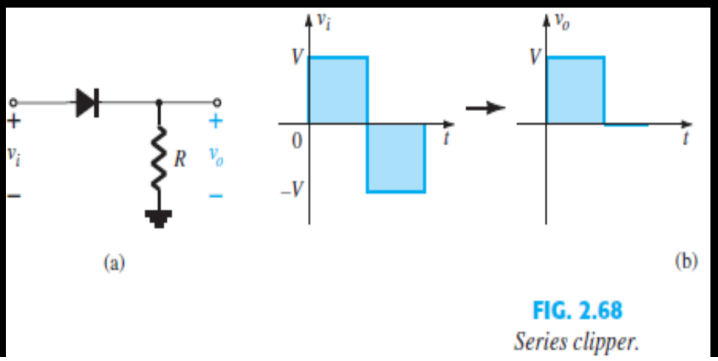
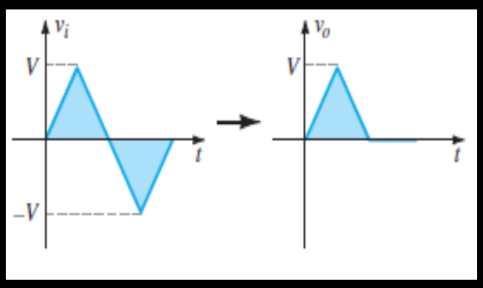


FIG. 2.68
Series clipper.



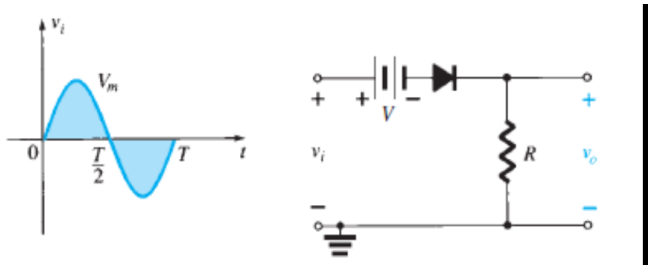


FIG. 2.69
Series clipper with a dc supply.

any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply V will oppose that applied voltage and try to keep the diode in the "off" state.

The result is that any supply voltage greater than V volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the diode will be on for any voltage vi that is greater than Vdc volts and off for any lesser voltage. For the "off" condition, the output would be 0 V due to the lack of current, and for the "on" condition it would simply be vo = vi - V as determined by Kirchhoff's voltage law.

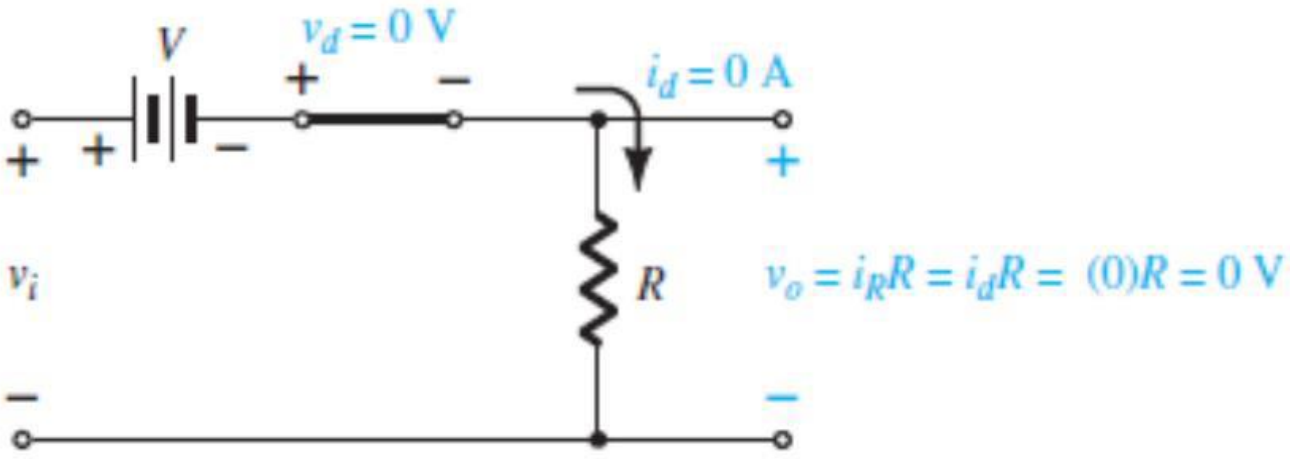


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

$$v_i = V$$

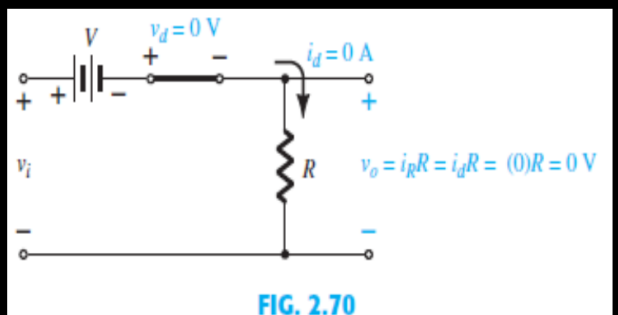


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

$$v_i = V$$

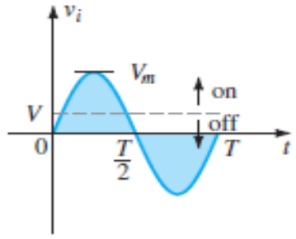


FIG. 2.71
Using the transition voltage to define the "on" and "off" regions.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20\text{ V}\ (0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$. For $v_i = -10\text{ V}$ the network of Fig. 2.79

Solution: For vi = 20 V (0 T/2) the network of Fig. 2.78 results. The diode is in the short-circuit state, and vo = 20 V + 5 V = 25 V.

For vi = -10 V the network of Fig. 2.79results, placing the diode in the "off" state, and vo = (iR R) = (0)R = 0 V. The resulting output voltage appears in Fig. 2.80

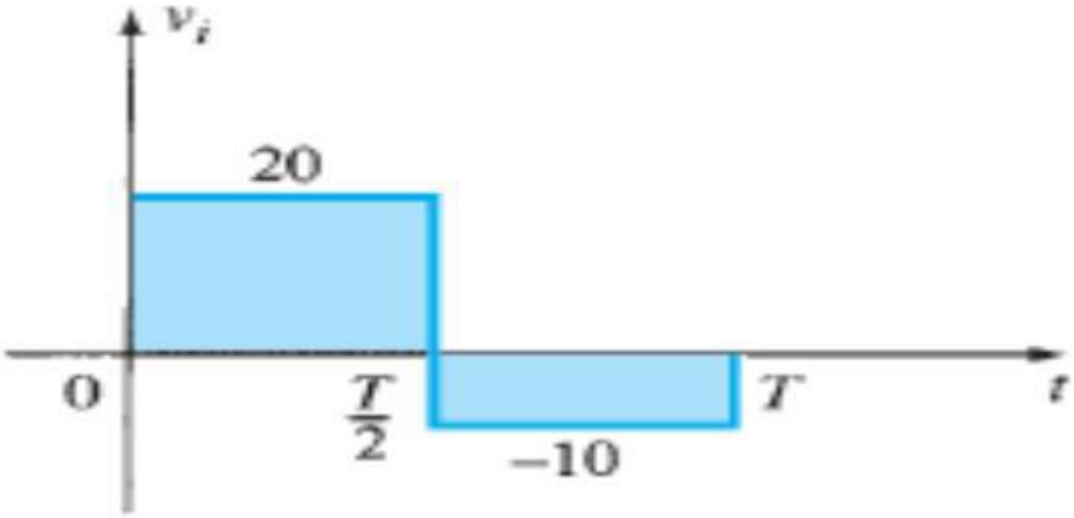


FIG. 2.77
Applied signal for Example 2.19.

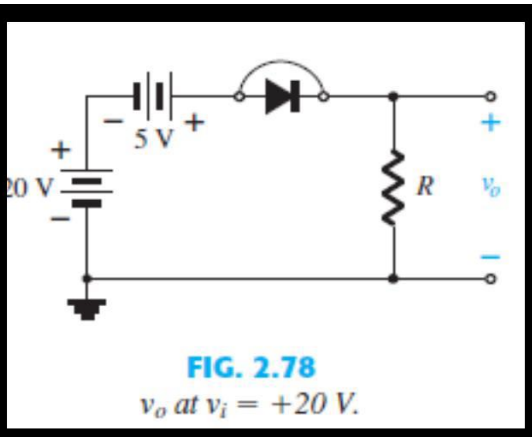


FIG. 2.78
v_o *at* $v_i = +20$ *V.*

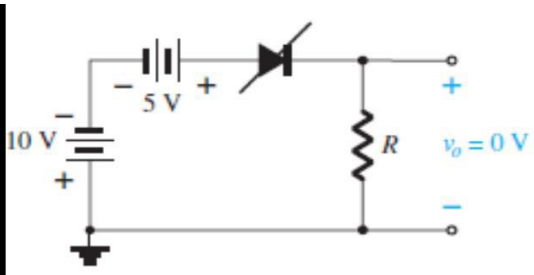


FIG. 2.79
v_o *at* $v_i = -10$ *V.*

Solution: For $v_i = 20$ V $(0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_0 = 20$ V + 5 V = 25 V. For $v_i = -10$ V the network of Fig. 2.79

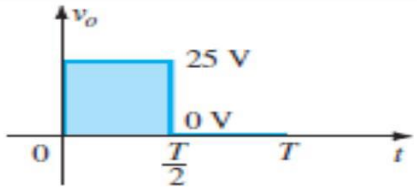
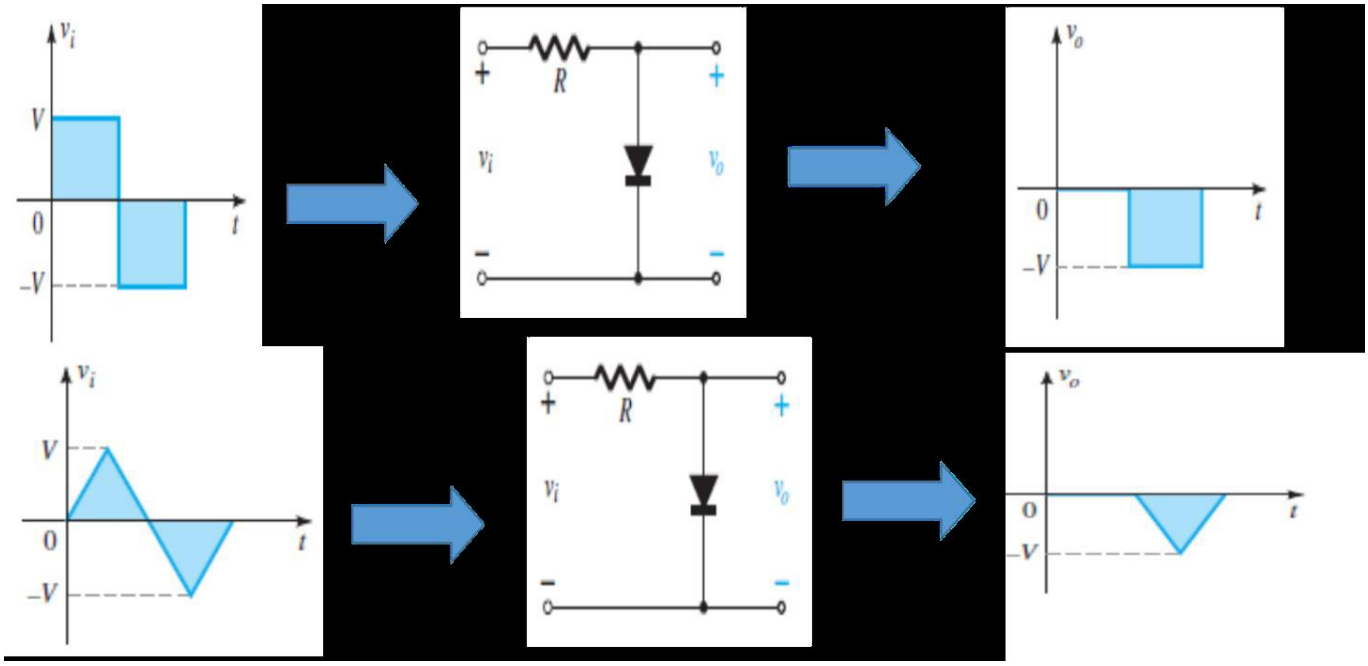


FIG. 2.80
Sketching v_o *for Example 2.19.*

Parallel



clamper

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal. Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

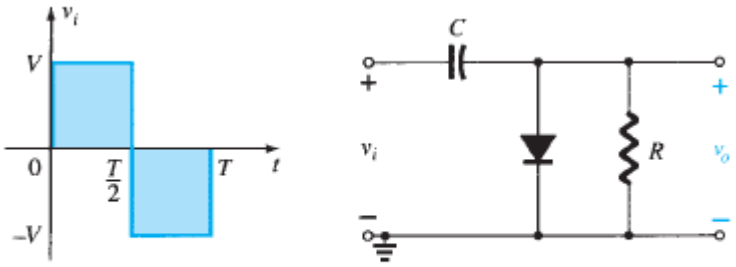


FIG. 2.89
Clamper.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode

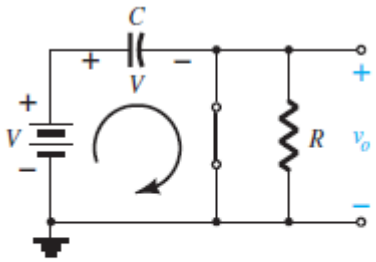


FIG. 2.90
Diode "on" and the capacitor charging to V volts.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v o to ensure that the proper levels are obtained.

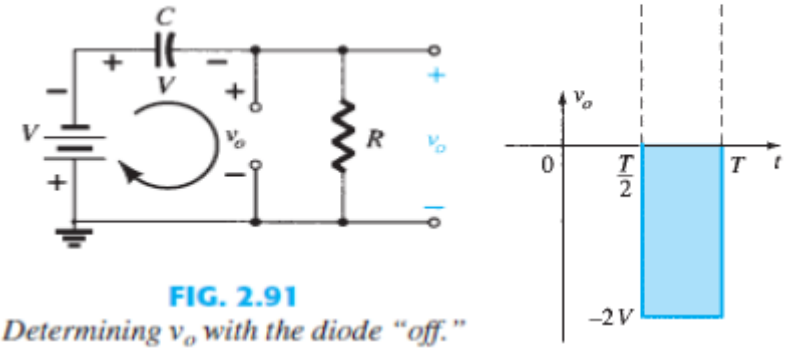


FIG. 2.91
Determining v_o with the diode "off."

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.

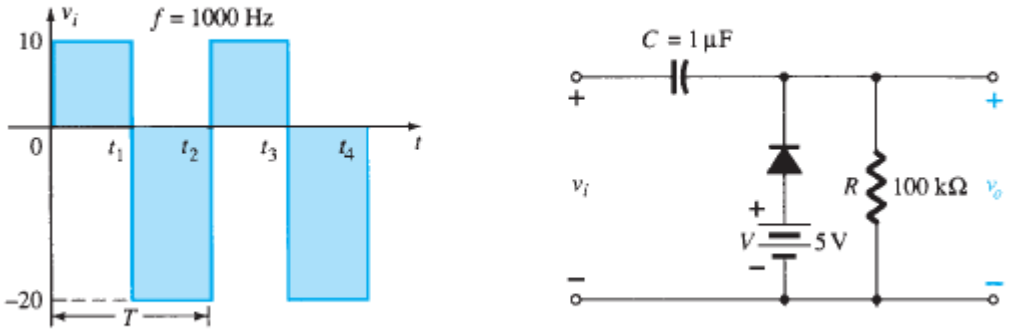


FIG. 2.93
Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an Interval of 0.5 ms between levels. The analysis will begin with the period t1 St2 of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94 . The output is across R , but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for vo and the battery terminals. The result is v o =5 V for this interval. Applying Kirchhoff's voltage law around the input loop results in.

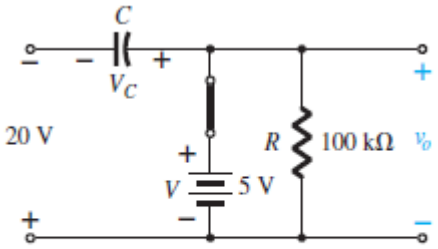


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.

$$-20\text{ V} + V_C - 5\text{ V} = 0$$
$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor *R* is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period *t*2 *t*3 the network will appear as shown in Fig. 2.95 . The opencircuit equivalent for the diode removes the 5-V battery from having any effect on *v o* , and applying Kirchhoff's voltage law around the outside loop of the network results in

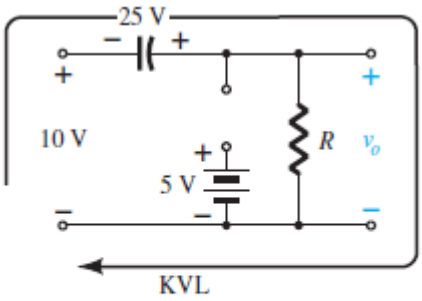


FIG. 2.95
Determining v_o with the diode in the "off" state.

$$+10\,\text{V} + 25\,\text{V} - v_o = 0$$
$$v_o = 35\,\text{V}$$

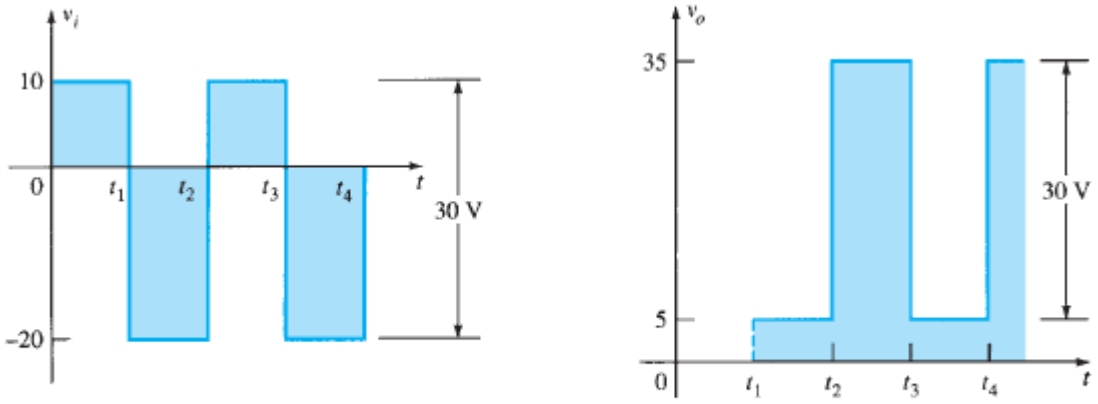


FIG. 2.96
v_i and v_o for the clamper of Fig. 2.93.

Clamping Networks

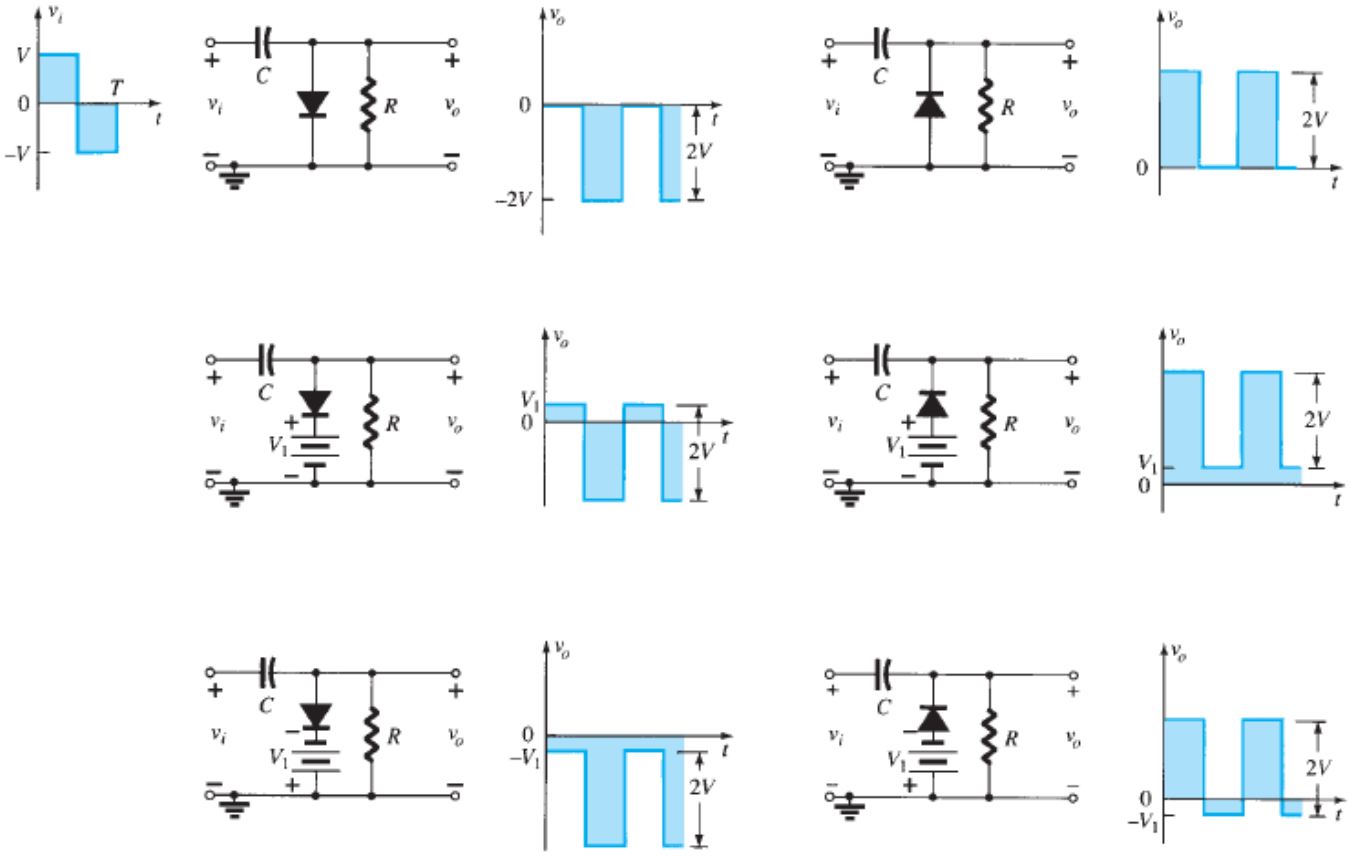


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

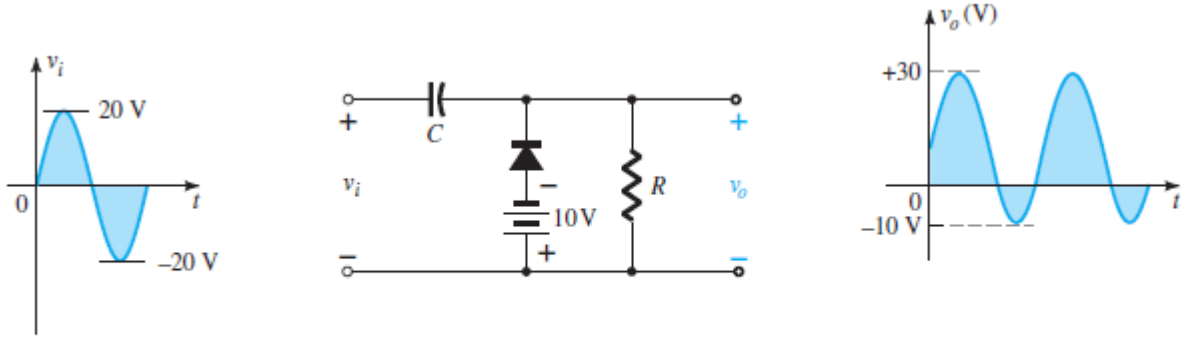


FIG. 2.101
Clamping network with a sinusoidal input.

الوحدة الثانية - المحاضرة الخامسة - الزمن: 120 دقيقة

أهداف المحاضرة:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

ماهو الزينر دايود وماهي خصائصه

موضوعات المحاضرة الثانية:

ZENER DIODES

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة سؤال وجواب اختبار	• جهاز حاسوب • جهاز عرض • سبورة اوراق واقلام

المادة العلمية:

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. **Zener diode can be used to establish reference voltage levels and act as a protection device. voltage reference** is an electronic device which produces a constant voltage regardless of the loading on the device, temperature changes, passage of time and power supply variations. The voltage reference circuit most commonly used in integrated circuits is the bandgap voltage referenc

EXAMPLE 2.24

Determine the reference voltages provided by the network of Fig. 2.109 , which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V,
for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

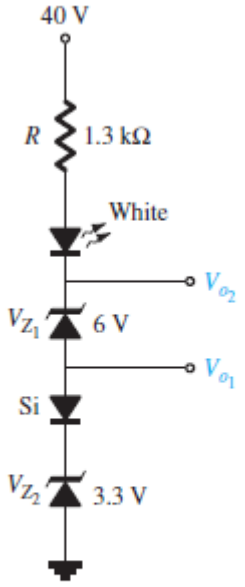


FIG. 2.109
Reference setting circuit for Example 2.24.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_2} + V_K = 3.3\text{ V} + 0.7\text{ V} = \mathbf{4.0\text{ V}}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4\text{ V} + 6\text{ V} = \mathbf{10\text{ V}}$$

Finally, the 4 V across the white LED will leave a voltage of 40 V – 14 V = 26 V across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40\text{ V} - V_{o_2} - V_{\text{LED}}}{1.3\text{ k}\Omega} = \frac{40\text{ V} - 10\text{ V} - 4\text{ V}}{1.3\text{ k}\Omega} = \frac{26\text{ V}}{1.3\text{ k}\Omega} = \mathbf{20\text{ mA}}$$

which should establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40\text{ V})(20\text{ mA}) = \mathbf{800\text{ mW}}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4\text{ V})(20\text{ mA}) = \mathbf{80\text{ mW}}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6\text{ V})(20\text{ mA}) = \mathbf{120\text{ mW}}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

Vi and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.112 . The applied dc voltage
is fixed, as is the load resistor. The analysis can fundamentally be broken down into
two steps.

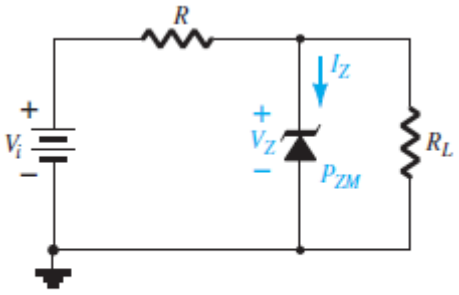


FIG. 2.112
Basic Zener regulator.

1. Determine the state of the **Zener diode by removing it** from the network andcalculating the voltage across the resulting
open circuit**.**

Applying step 1 to the network of Fig. 2.112 results in the network of Fig. 2.113 ,

wherean application of the voltage divider rule results in

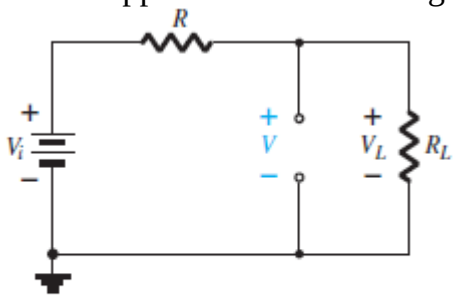


FIG. 2.113
Determining the state of the Zener diode.

$$V = V_L = \frac{R_L V_i}{R + R_L}$$

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.
If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.112, the "on" state will result in the equivalent network of Fig. 2.114. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

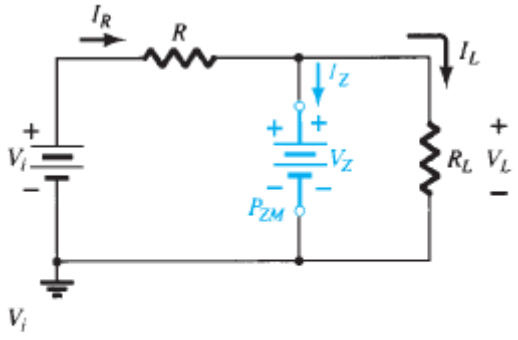


FIG. 2.114
Substituting the Zener equivalent for the "on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

EXAMPLE 2.26

a. For the Zener diode network of Fig. 2.115, determine V_L, V_R, I_Z, and P_Z.
b. Repeat part (a) with $R_L = 3\,\text{k}\Omega$.

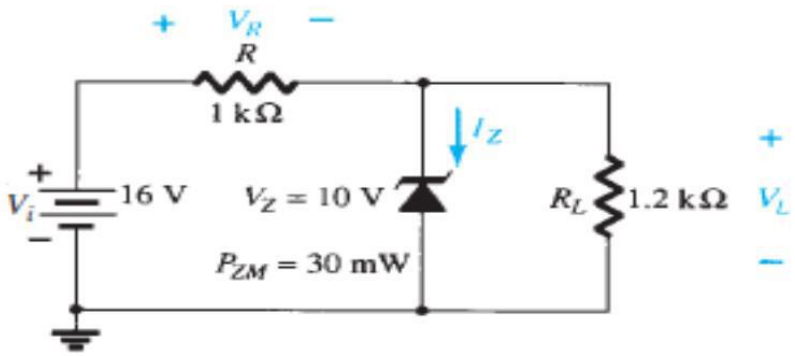


FIG. 2.115
Zener diode regulator for Example 2.26.

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.116. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 1.2\,\text{k}\Omega} = 8.73\,\text{V}$$

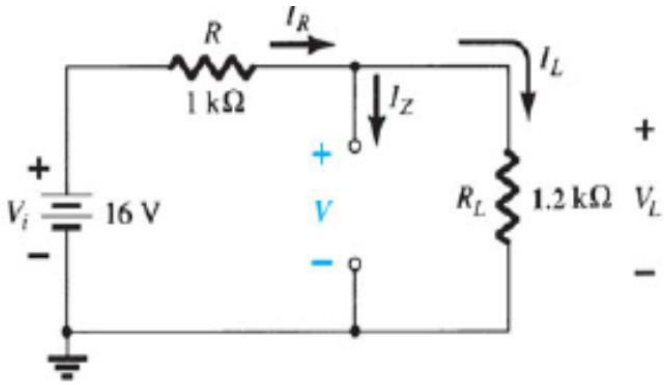


FIG. 2.116
Determining V for the regulator of Fig. 2.115.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state, as shown on the characteristics of Fig. 2.117. Substituting the open-circuit equivalent results in the same network as in Fig. 2.116, where we find that

$$V_L = V = \mathbf{8.73\ V}$$
$$V_R = V_i - V_L = 16\ \text{V} - 8.73\ \text{V} = \mathbf{7.27\ V}$$
$$I_Z = \mathbf{0\ A}$$

and
$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the work of Fig. 2.118 results. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and
$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with
$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and
$$I_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that
$$I_Z = I_R - I_L\ [\text{Eq. (2.18)}]$$
$$= 6\ \text{mA} - 3.33\ \text{mA}$$
$$= \mathbf{2.67\ mA}$$

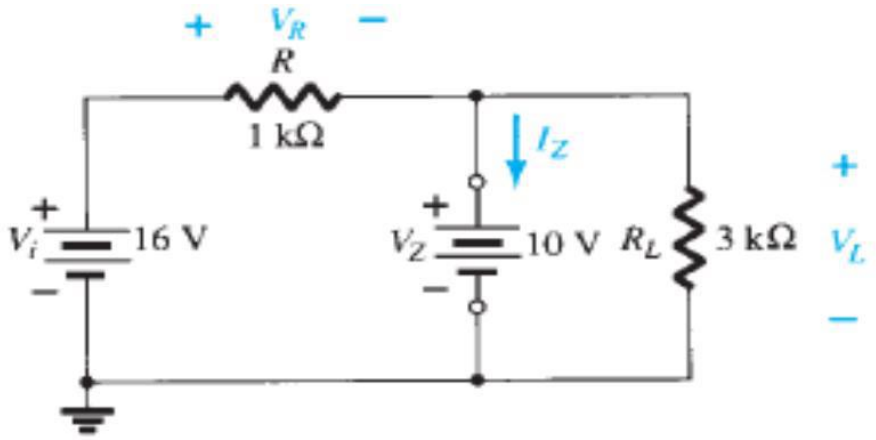


FIG. 2.118
Network of Fig. 2.115 in the "on" state.

The power dissipated is

$$P_Z = V_Z I_Z = (10\text{ V})(2.67\text{ mA}) = \mathbf{26.7\text{ mW}}$$

which is less than the specified $P_{ZM} = 30$ mW.

Fixed Vi , Variable RL

Due to the offset voltage V Z , there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R L will result in a voltage V L across the load resistor less than V Z , and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.112 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \qquad \textbf{(2.20)}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L, but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \qquad \textbf{(2.21)}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

a. For the network of Fig. 2.119, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
b. Determine the maximum wattage rating of the diode.

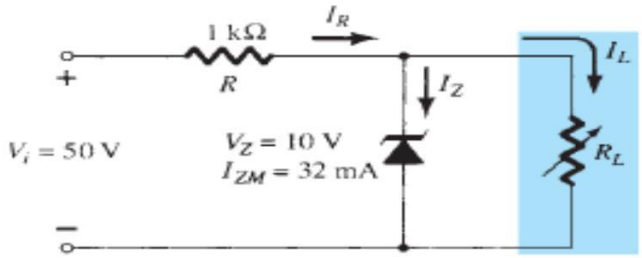


FIG. 2.119
Voltage regulator for Example 2.27.

Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\text{ V}}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\text{ mA}}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\text{ mA}}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\text{ k}\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.120a and for V_L versus I_L in Fig. 2.120b.

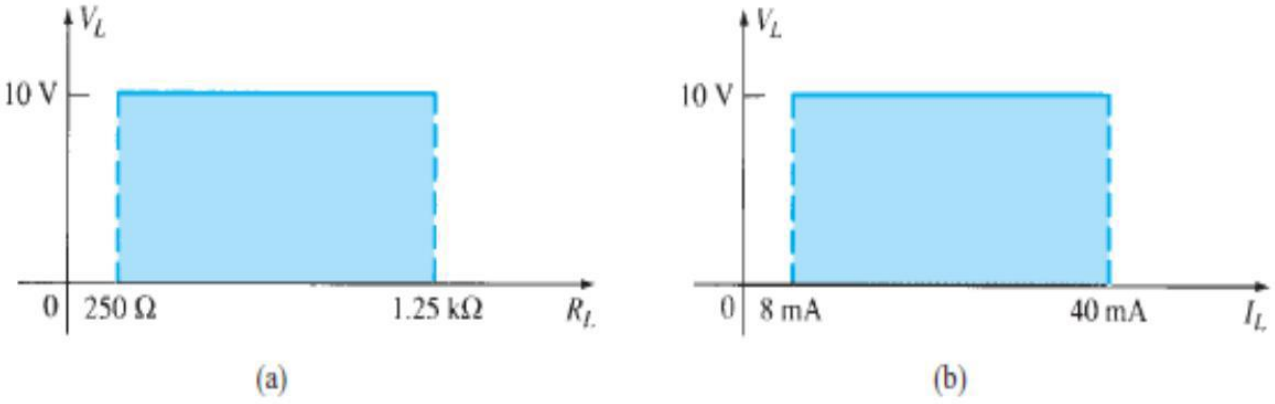


FIG. 2.120

V_L versus R_L and I_L for the regulator of Fig. 2.119.

b. $P_{max} = V_Z I_{ZM}$

$= (10\text{ V})(32\text{ mA}) = \mathbf{320\text{ mW}}$

الوحدة الثالثة - المحاضرة السادسة - الزمن: 120 دقيقة

أهداف المحاضرة:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

1. Become familiar with the basic construction and operation of the Bipolar Junction Transistor.
2. Be able to apply the proper biasing to insure operation in the active region.

3. Recognize and be able to explain the characteristics of an npn or pnp transistor.

موضوعات المحاضرة الثانية:

1. definition of the Bipolar Junction Transistor.
2. Understand the characteristics of an npn or pnp transistor.
.3. apply the proper biasing to insure operation in the active region

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

3.1 INTRODUCTION

During the period 1904 to1947, the vacuum tube was the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third
66
element, called the control grid, to the vacuum diode, resulting in the first amplifier, the triode. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four element tetrode and the five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance, and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization. On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Dr. S. William Shockley, Walter H. Brattain, and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories as shown in Fig. 3.1 . The original transistor (a point-contact transistor) is shown in Fig. 3.2 . The advantages of this three-terminal solid-state device over the tube were immediately obvious:
It was smaller and lightweight; it had no heater requirement or heater loss; it had a rugged construction; it was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) have at least three terminals, with one controlling the flow or potential between the other two.

3.2-Transistor construction

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an NPN transistor, while the latter is called a PnP transistor. Transistor composed from

3.2.1-The emitter layer is heavily doped

3.2.2- The base lightly doped

3.2.3-The collector only lightly doped

This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of “free” carriers

The outer layers have widths much greater than the sandwiched p - or n -type material

The terminals have been indicated by the capital letters **E** for emitter, **C** for collector, and **B** for base, the term bipolar reflects the fact that holes and electrons participate in the

injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device.

3.3 TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the pnp transistor of Fig. 3.2a. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.3 the pnp transistor has been redrawn without the base-to-collector bias. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p- to the n-type material.

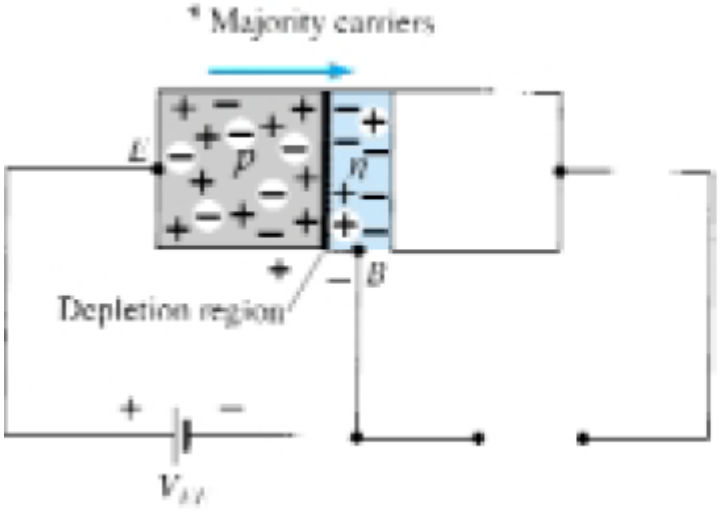

Figure 3.3 Forward-biased junction of a *pnp* transistor.

Let us now remove the base-to-emitter bias of the pnp transistor of Fig. 3.2a as shown in Fig. 3.4.. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.4. In summary, therefore:

One p-n junction of a transistor is reverse biased, while the other is forward biased.

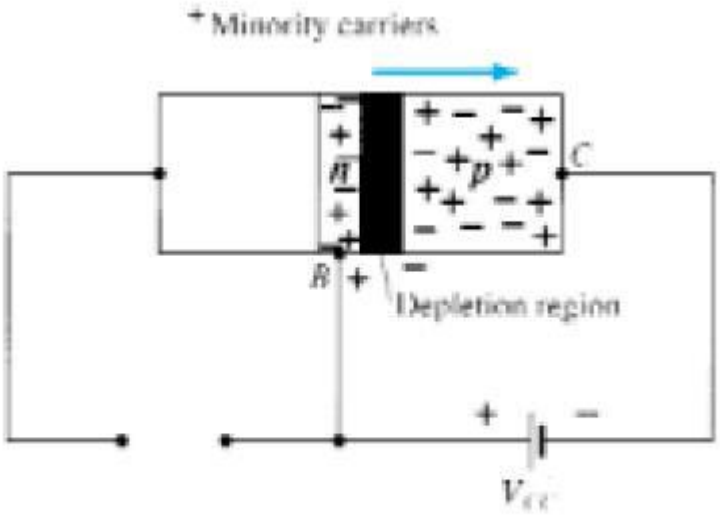

Figure 3.4 Reverse-biased junction of a *pnp* transistor.

In Fig. 3.5 both biasing potentials have been applied to a pnp transistor, with the resulting majority- and minority-carrier flow indicated. Note in Fig. 3.5 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.5, a large number of majority carriers will diffuse across the forward-biased p-n junction into the n-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the p-type material. Since the sandwiched n-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes as compared to mill amperes for the emitter and collector currents.

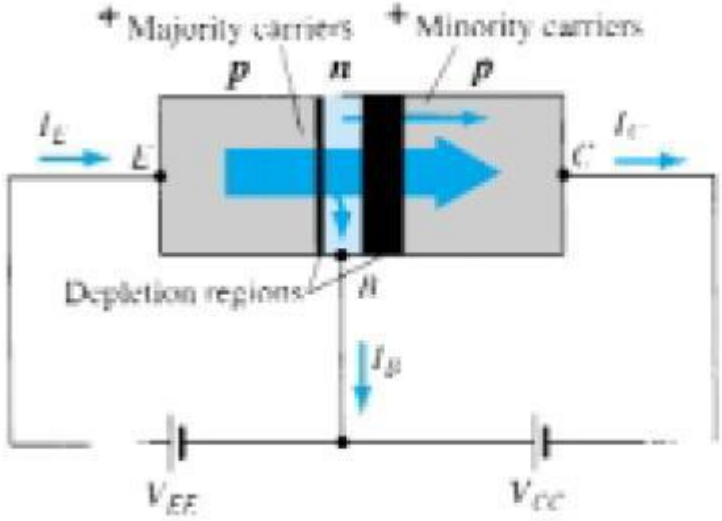

Figure 3.5 Majority and minority carrier flow of a *pnp* transistor.

Applying Kirchhoff's current law to the transistor of Fig. 3.5 as if it were a single node, we obtain

$$I_E = I_C + I_B \qquad (3.1)$$

The majority and minority carriers as indicated in Fig. 3.5. The minority-current component is called the leakage current and is given the symbol **ICO** (**IC** current with emitter terminal Open). The collector current, therefore, is determined in total by Eq. (3.2).

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}} \qquad (3.2)$$

For general-purpose transistors, **IC** is measured in milliamperes, while **ICO** is measured in microamperes or nanoamperes. **ICO**, like is for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of **ICO**, to the point where its effect can often be ignored.

1- Emitter-Base – forward bias junction

2- Collector-base– reverse bias junction

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أهداف المحاضرة:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

التعرف على مزايا BJT transistor characteristics

موضوعات المحاضرة الثانية:

BJT transistor characteristics

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الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

3.8 COMMON-COLLECTOR CONFIGURATIO) المشترك الجامع ترانزستور(

The third and final transistor configuration is the common-collector configuration, shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector (purposes since it has توفيق الممانعةconfiguration is used primarily for impedance-matching) a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

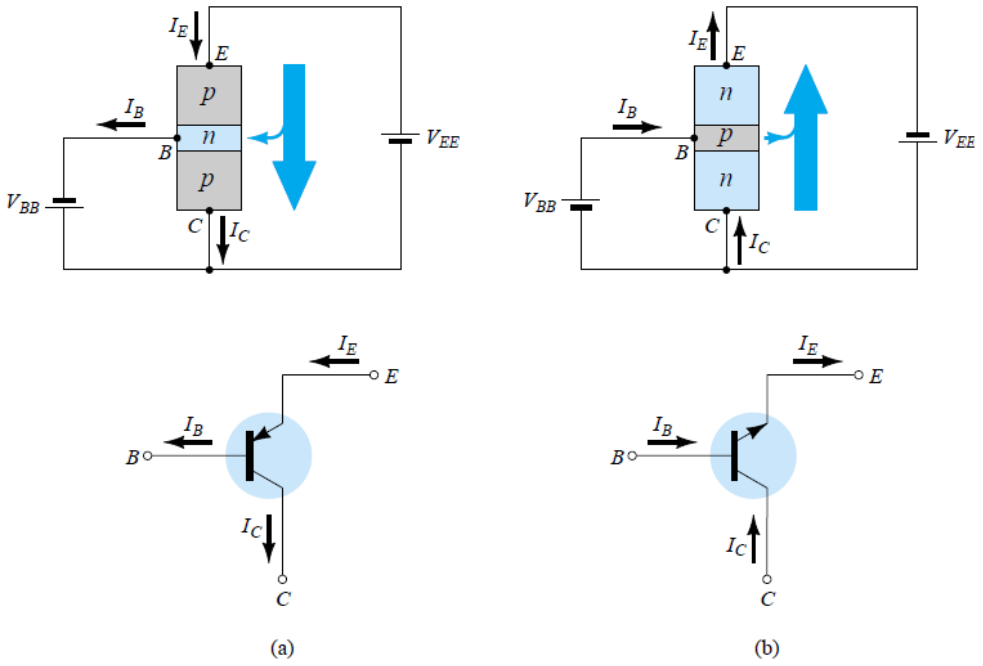

Figure 3.20 Notation and symbols used with the common-collector configuration: (a) *pnp* transistor; (b) *npn* transistor.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need

85

for a set of common collector characteristics to choose the parameters of the circuit of Fig.3.2 It can be designed using the common-emitter characteristics of Section 3.6

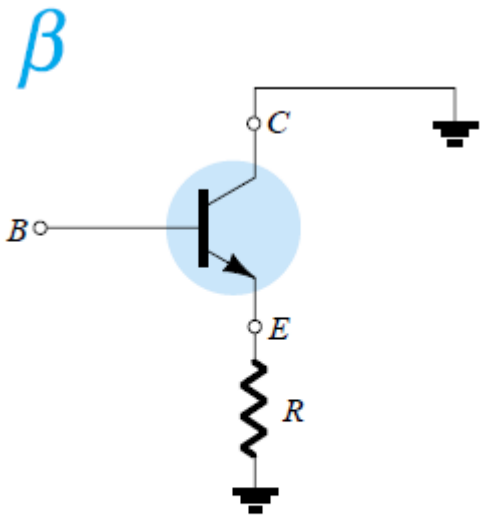

Figure 3.21 Common-collector configuration used for impedance-matching purposes.

For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{EC} for a range of values of I_B.

.The input current, therefore, is the same for both the common-emitter and common collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information

3.9 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics which will ensure))يضمن that the maximum ratings are not being exceeded)يتجاوز(

(. Such a region has been اقل تشويه and the output signal exhibits minimum distortion) defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as continuous collector current) and maximum collector-to-emitter voltage (often abbreviated as V_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, I_{Cmax} was specified as 50 mA and V_{CEO} as 20 V. The vertical line on the characteristics defined as VCEsat specifies

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أهداف المحاضرة:

يتوقع في نهاية الجلسة أن يكون الطالب قادراً على:

1 Be able to determine the dc levels for the variety of important BJT configurations.
2 Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.

موضوعات المحاضرة الثانية:

Dc biasing- BJT

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الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

4.1 INTRODUCTION •

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.
The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.

The following important basic relationships for a transistor:

$$V_{BE} \cong 0.7\ \text{V} \tag{4.1}$$

$$I_E = (\beta + 1)I_B \cong I_C \tag{4.2}$$

$$I_C = \beta I_B \tag{4.3}$$

4.2 OPERATING POINT

The term biasing appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

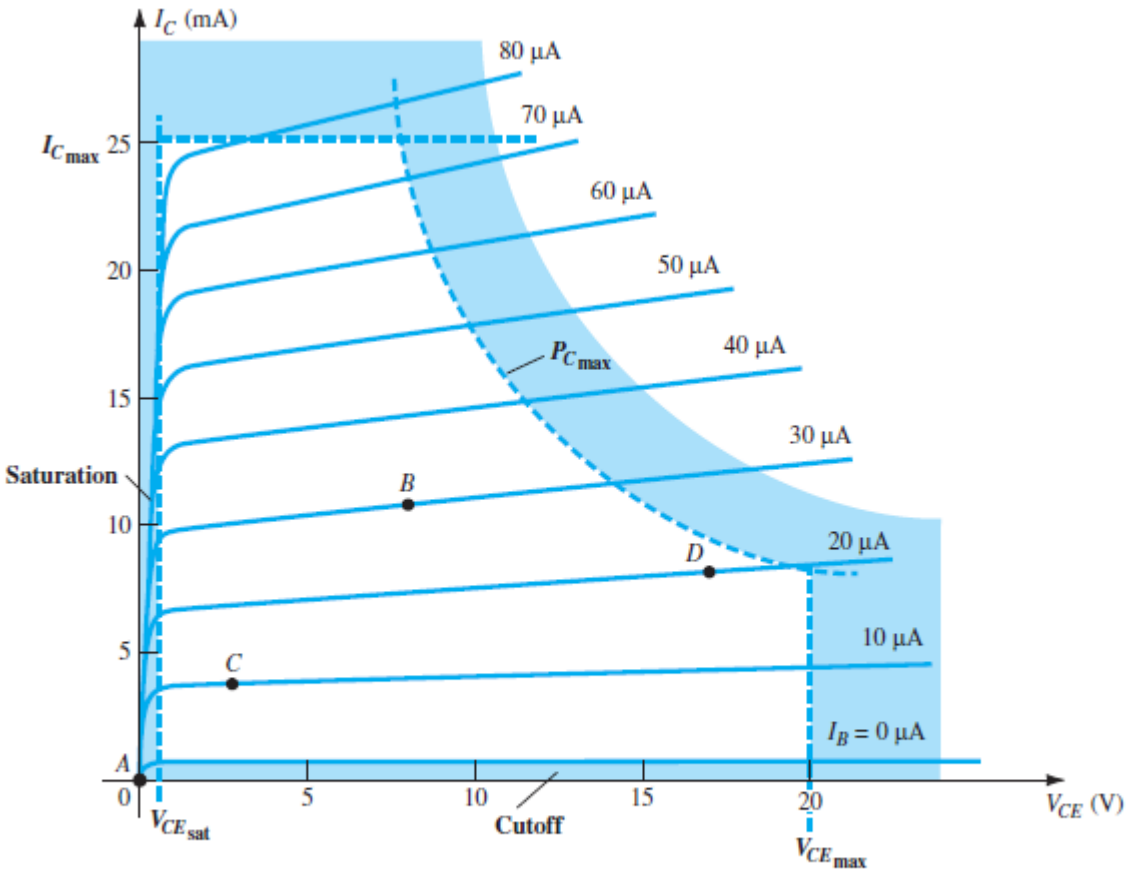

FIG. 4.1
Various operating points within the limits of operation of a transistor.

For the BJT to be biased in its linear or active operating region the following must be true:
1. *The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.*
*2. The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device***.**
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[Note that for forward bias the voltage across the p–n junction is p - p
ositive, whereas for reverse bias it is opposite (reverse) with n -positive.]
Operation in the cutoff, saturation, and linear regions of the BJT
characteristic are providedas follows:

1. Linear-region operation:
Base–emitter junction forward-biased
Base–collector junction reverse-biased
2. Cutoff-region operation:
Base–emitter junction reverse-biased
Base–collector junction reverse-biased
3. Saturation-region operation:

Base–emitter junction forward-biased
Base–collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration.

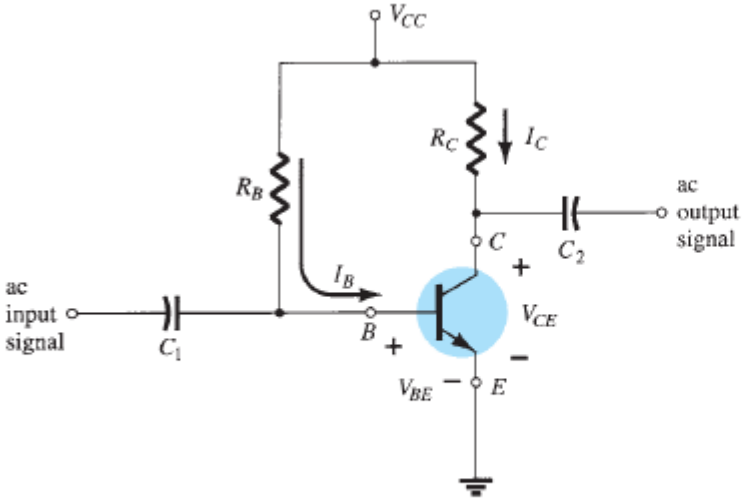

FIG. 4.2
Fixed-bias circuit.

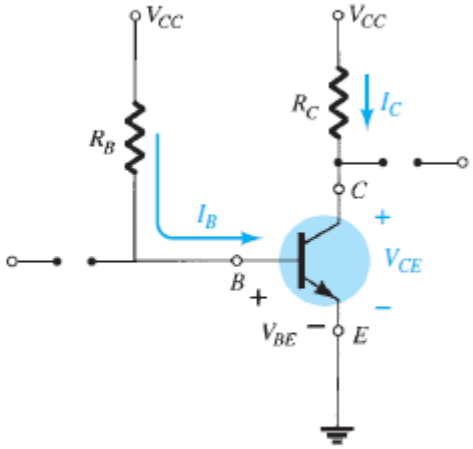

FIG. 4.3
DC equivalent of Fig. 4.2.

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موضوعات المحاضرة:

DC analysis of BJT transistor

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4.4 EMITTER-BIAS CONFIGURATION

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.18 can be redrawn as shown in Fig. 4.19. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad \textbf{(4.15)}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \qquad \textbf{(4.16)}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \qquad \textbf{(4.17)}$$

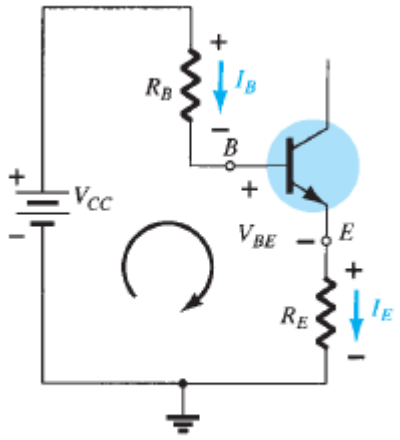

FIG. 4.19
Base–emitter loop.

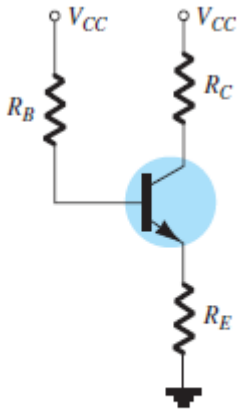

FIG. 4.18
DC equivalent of Fig. 4.17.

Collector–Emitter Loop

The collector–emitter loop appears in Fig. 4.22. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad (4.19)$$

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23 , determine: a. I_B . b. I_C . c. V_{CE} . d. V_C . e. V_E . f. V_B . g.V_{BC} .

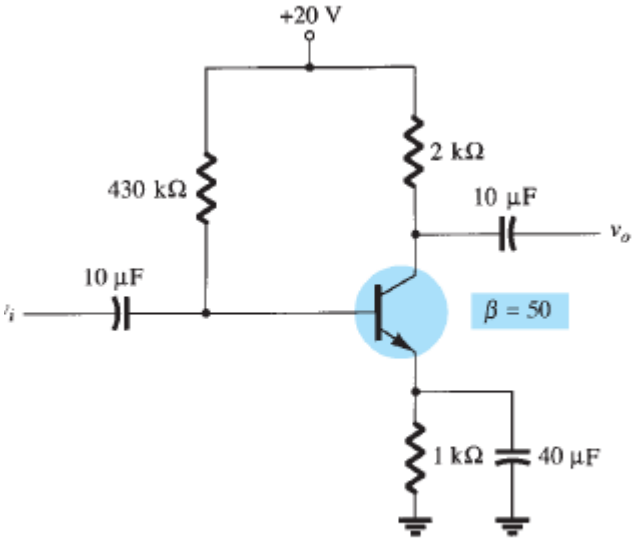

FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\,\text{k}\Omega + (51)(1\,\text{k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\,\text{k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\,\text{k}\Omega + 1\,\text{k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\ V}$

d. $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\,\text{k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\ V}$

e. $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\,\text{k}\Omega)$
$= \mathbf{2.01\ V}$

f. $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\ V}$

g. $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\ V}$ (reverse-biased as required)

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موضوعات المحاضرة الثانية:

VOLTAGE-DIVIDER BIAS CONFIGURATION

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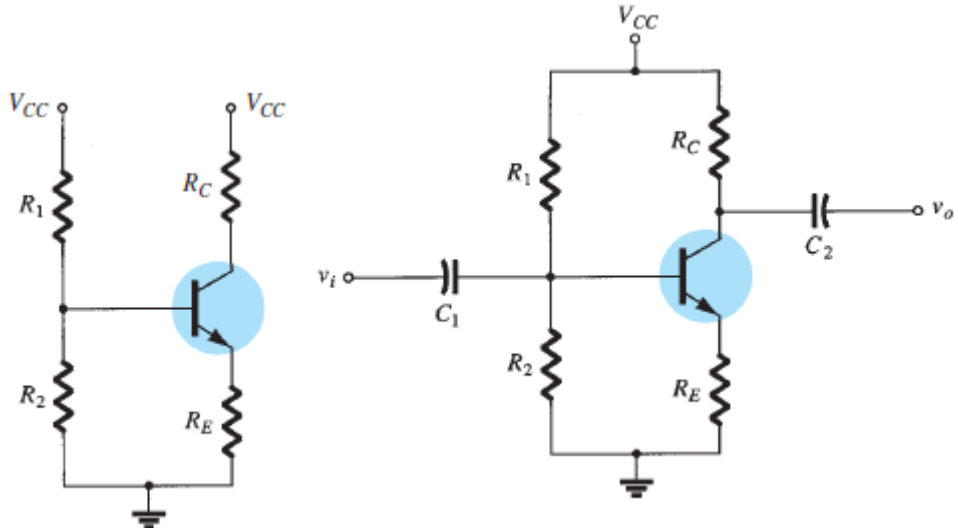
4.5 VOLTAGE-DIVIDER BIAS CONFIGURATION



Exact Analysis

R_{Th} The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.32

$$R_{Th} = R_1 \| R_2$$

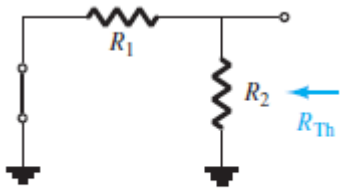


FIG. 4.32
Determining R_{Th}.

E_{Th} The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.33 determined as
follows:
Applying the voltage-divider rule gives

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

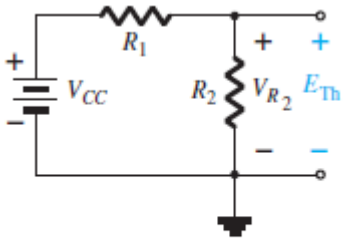


FIG. 4.33
Determining E_{Th}.

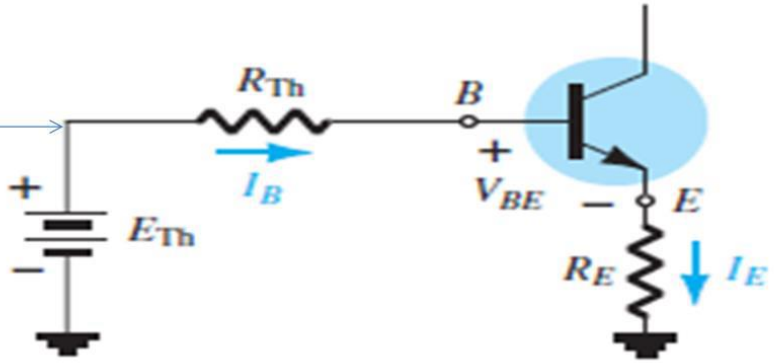
applying Kirchhoff's voltage law in the clockwise direction

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

g $I_E = (\beta + 1) I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

The Thévenin network is then **redrawn** as shown in Fig.



$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

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موضوعات المحاضرة الثانية:

DC analysis of BJT transistor

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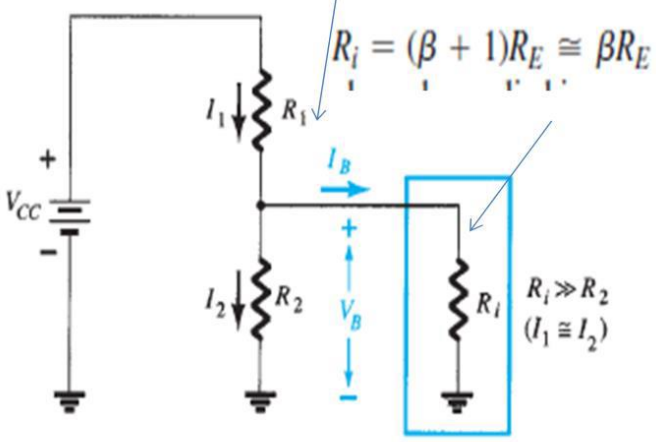
Approximate Analysis

Because $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied is

$$\beta R_E \geq 10R_2$$

IB will be much smaller than I2

I2



then I1 = I2, and R1 and R2 can be considered series elements. The voltage across R2 , which is actually the base voltage

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

FIG. 4.36
Partial-bias circuit for calculating the approximate base voltage V_B.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

and

$$I_{C_Q} \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

EXAMPLE 4.9 Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

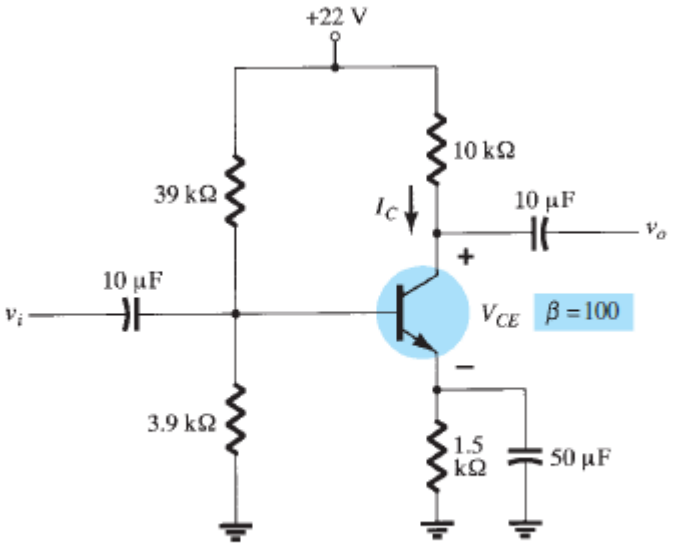


FIG. 4.35
Beta-stabilized circuit for Example 4.8.

Solution: Testing:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\,\text{k}\Omega) \geq 10(3.9\,\text{k}\Omega)$$
$$150\,\text{k}\Omega \geq 39\,\text{k}\Omega \ (\textit{satisfied})$$

$$\text{Eq. (4.32):} \quad V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7 . Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B .

$$\text{Eq. (4.34):} \quad V_E = V_B - V_{BE} = 2\,\text{V} - 0.7\,\text{V} = 1.3\,\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\,\text{V}}{1.5\,\text{k}\Omega} = \mathbf{0.867\,mA}$$

compared to 0.84 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.867\,\text{mA})(10\,\text{kV} + 1.5\,\text{k}\Omega) = 22\,\text{V} - 9.97\,\text{V} = \mathbf{12.03\,V}$$

The results for I_{CQ} and V_{CEQ} are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of Ri compared to R2 , the closer is the

approximate to the exact solution. Example 4.11 will compare solutions at a level well below the condition established by Eq. (4.33).

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.25, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\,\text{V}} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0\,\text{mA}} \tag{4.40}$$

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

$I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

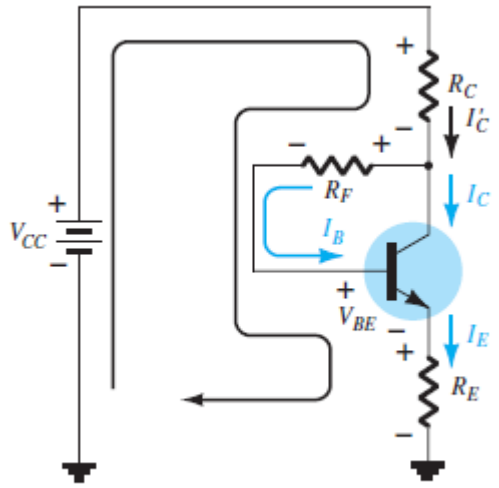


FIG. 4.39

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

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Emitter Loop

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EXAMPLE 4.12 Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.41.

Solution: Eq. (4.41): $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\text{ mA}}$$

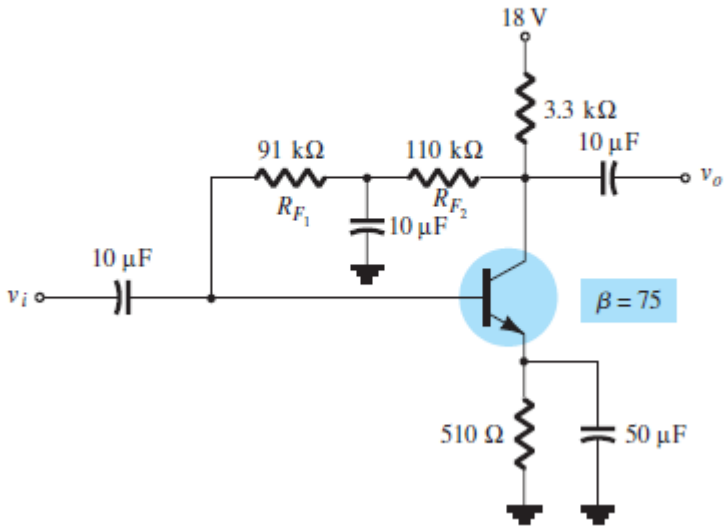
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

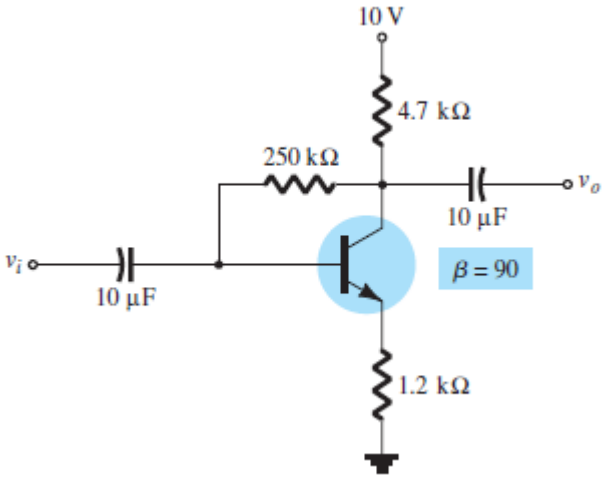
$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\text{ V}}$$

EXAMPLE 4.14 Determine the dc level of I_B and V_C for the network of Fig. 4.42.





Solution: In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and $R_B = R_{F_1} + R_{F_2}$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\text{ k}\Omega + 110\text{ k}\Omega) + (75)(3.3\text{ k}\Omega + 0.51\text{ k}\Omega)}$$

$$= \frac{17.3\text{ V}}{201\text{ k}\Omega + 285.75\text{ k}\Omega} = \frac{17.3\text{ V}}{486.75\text{ k}\Omega}$$

$$= \mathbf{35.5\ \mu A}$$

$$I_C = \beta I_B$$
$$= (75)(35.5\ \mu A)$$
$$= 2.66\ mA$$
$$V_C = V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C$$
$$= 18\ V - (2.66\ mA)(3.3\ k\Omega)$$
$$= 18\ V - 8.78\ V$$
$$= \mathbf{9.22\ V}$$

Saturation Conditions

Using the approximation $I'_C = I_C$, we find that the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ results in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} is defined by the chosen bias configuration.

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Applying Kirchhoff's voltage law to the entire outside perimeter of the network of Fig. 4.51 will result in

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

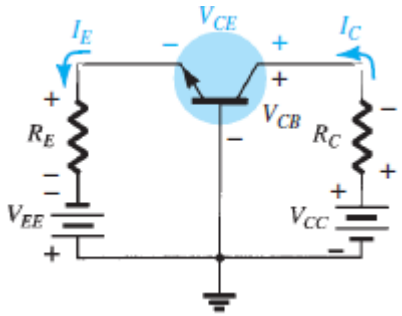
and solving for V_{CE}:

$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

Because

$$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)} \qquad (4.47)$$



The voltage V_{CB} of Fig. 4.51 can be found by applying Kirchhoff's voltage law to the output loop of Fig 4.51 to obtain:

$$V_{CB} + I_C R_C - V_{CC} = 0$$

or
$$V_{CB} = V_{CC} - I_C R_C$$

Using
$$I_C \cong I_E$$

we have
$$\boxed{V_{CB} = V_{CC} - I_C R_C} \qquad (4.48)$$

EXAMPLE 4.17 Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of Fig. 4.52.

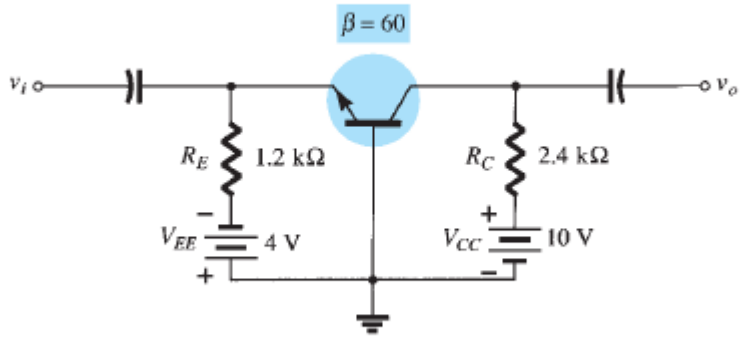


FIG. 4.52
Example 4.17.

Solution: Eq. 4.46:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.75\text{ mA}}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{ mA}}{60 + 1} = \frac{2.75\text{ mA}}{61}$$

$$= \mathbf{45.08\ \mu A}$$

Eq. 4.47:

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$

$$= 4\text{ V} + 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 14\text{ V} - (2.75\text{ mA})(3.6\text{ k}\Omega)$$

$$= 14\text{ V} - 9.9\text{ V}$$

$$= \mathbf{4.1\text{ V}}$$

Eq. 4.48:

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= 10\text{ V} - (60)(45.08\ \mu\text{A})(24\text{ k}\Omega)$$

$$= 10\text{ V} - 6.49\text{ V}$$

$$= \mathbf{3.51\text{ V}}$$

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موضوعات المحاضرة الثانية:

AC analysis of BJT transistor

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المادة العلمية:

MISCELLANEOUS BIAS CONFIGURATIONS

EXAMPLE 4.20 Determine V_C and V_B for the network of Fig. 4.55.

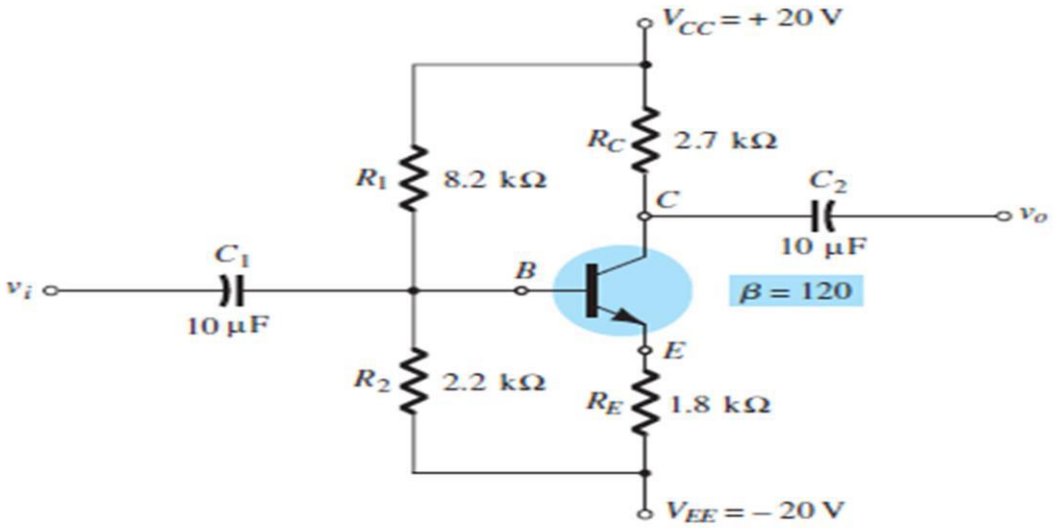

FIG. 4.55
Example 4.20.

Solution: The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.56 and 4.57.

R_{Th}

$$R_{Th} = 8.2\,\text{k}\Omega \,\|\, 2.2\,\text{k}\Omega = 1.73\,\text{k}\Omega$$

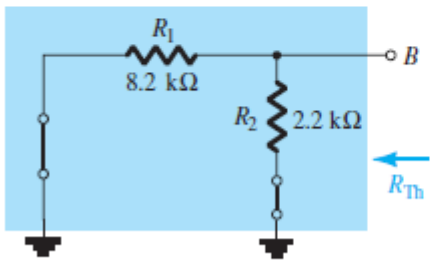

FIG. 4.56
Determining R_{Th}.

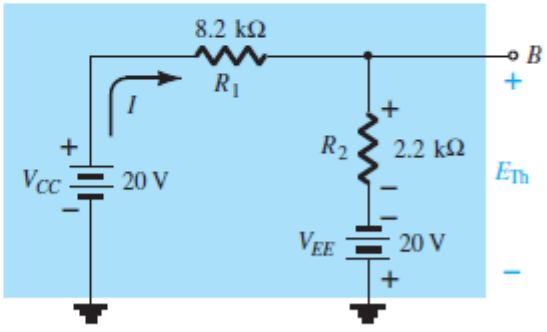

FIG. 4.57
Determining E_{Th}.

E_{Th}

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\text{ V} + 20\text{ V}}{8.2\,\text{k}\Omega + 2.2\,\text{k}\Omega} = \frac{40\text{ V}}{10.4\,\text{k}\Omega}$$
$$= 3.85\text{ mA}$$
$$E_{Th} = IR_2 - V_{EE}$$
$$= (3.85\text{ mA})(2.2\,\text{k}\Omega) - 20\text{ V}$$
$$= -11.53\text{ V}$$

The network can then be redrawn as shown in Fig. 4.58, where the application of Kirchhoff's voltage law results in

$$-E_{Th} - I_BR_{Th} - V_{BE} - I_ER_E + V_{EE} = 0$$

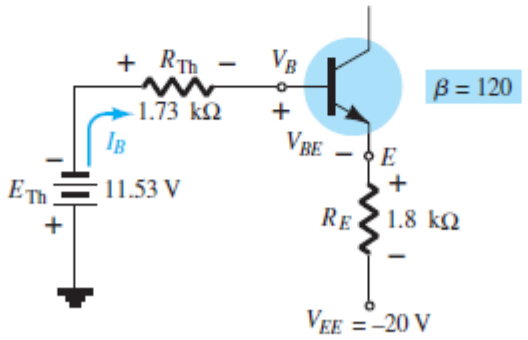

FIG. 4.58
Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_BR_E - I_BR_{Th} = 0$$

and

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{20\text{ V} - 11.53\text{ V} - 0.7\text{ V}}{1.73\,\text{k}\Omega + (121)(1.8\,\text{k}\Omega)}$$
$$= \frac{7.77\text{ V}}{219.53\,\text{k}\Omega}$$
$$= 35.39\,\mu\text{A}$$
$$I_C = \beta I_B$$
$$= (120)(35.39\,\mu\text{A})$$
$$= 4.25\text{ mA}$$
$$V_C = V_{CC} - I_CR_C$$
$$= 20\text{ V} - (4.25\text{ mA})(2.7\,\text{k}\Omega)$$
$$= \mathbf{8.53\text{ V}}$$
$$V_B = -E_{Th} - I_BR_{Th}$$
$$= -(11.53\text{ V}) - (35.39\,\mu\text{A})(1.73\,\text{k}\Omega)$$
$$= \mathbf{-11.59\text{ V}}$$

EXAMPLE 4.18

For the network of Fig. 4.53 : a. Determine I_{CQ} and V_{CEQ}. b. Find V_B, V_C, V_E, and V_{BC}.

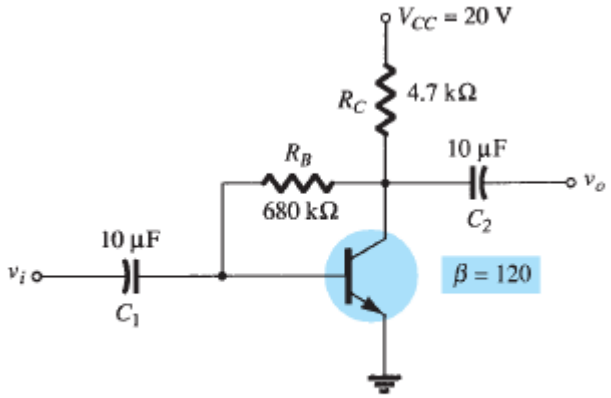

FIG. 4.53
Collector feedback with $R_E = 0\ \Omega$.

Solution:

a. The absence of R_E reduces the reflection of resistive levels to simply that of R_C, and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$= \frac{20\ \text{V} - 0.7\ \text{V}}{680\ \text{k}\Omega + (120)(4.7\ \text{k}\Omega)} = \frac{19.3\ \text{V}}{1.244\ \text{M}\Omega}$$

$$= \mathbf{15.51\ \mu A}$$

$$I_{C_Q} = \beta I_B = (120)(15.51\ \mu\text{A})$$

$$= \mathbf{1.86\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$

$$= 20\ \text{V} - (1.86\ \text{mA})(4.7\ \text{k}\Omega)$$

$$= \mathbf{11.26\ V}$$

b.

$$V_B = V_{BE} = \mathbf{0.7\ V}$$

$$V_C = V_{CE} = \mathbf{11.26\ V}$$

$$V_E = \mathbf{0\ V}$$

$$V_{BC} = V_B - V_C = 0.7\ \text{V} - 11.26\ \text{V}$$

$$= \mathbf{-10.56\ V}$$

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موضوعات المحاضرة:

MULTIPLE BJT NETWORKS

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المادة العلمية:

MULTIPLE BJT NETWORKS

The BJT networks introduced thus far have only been single-stage configurations. This section will cover some of the most popular networks using multiple transistors. It will
demonstrate how the methods introduced thus far in this chapter can be applied to networks with any number of components.

The R–C coupling of Fig. 4.64 is probably the most common. The collector output of one stage is fed directly into the base of the next stage using a coupling capacitor *C C* . The capacitor
is chosen to ensure that it will block dc between the stages and act like a short circuit to any ac signal.

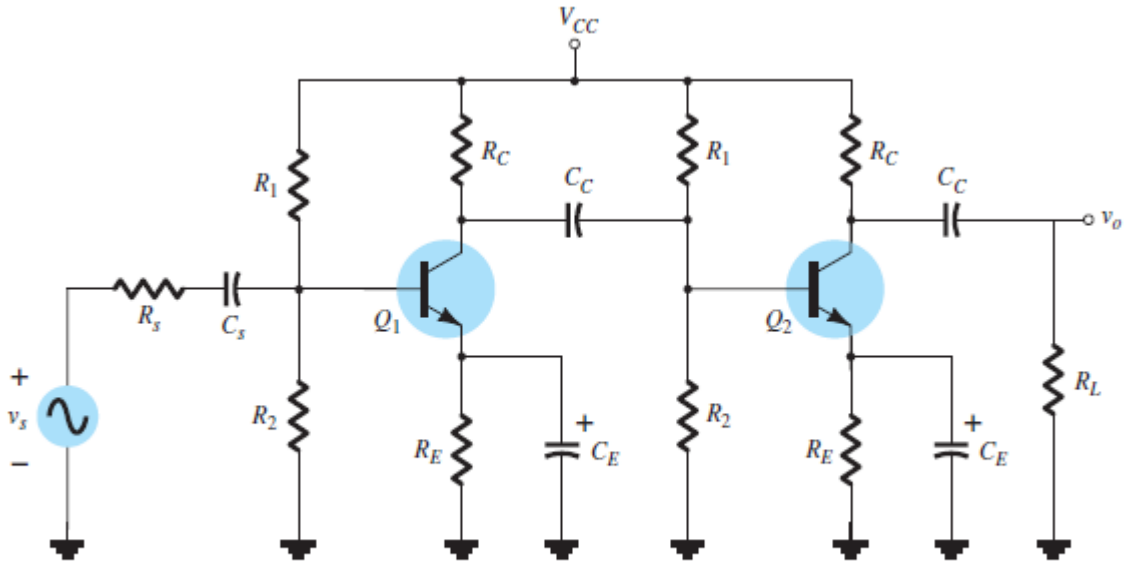


FIG. 4.64
R–C coupled BJT amplifiers.

Darlington configuration

The Darlington configuration of Fig. 4.66 feeds the output of one stage directly into the input of the succeeding stage. Since the output of Fig. 4.66 is taken directly off the emitter terminal.

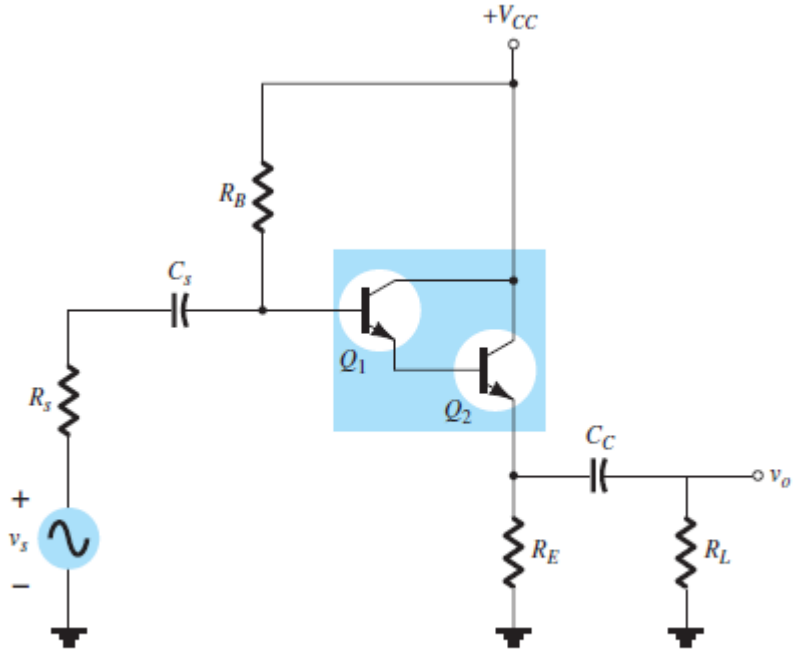
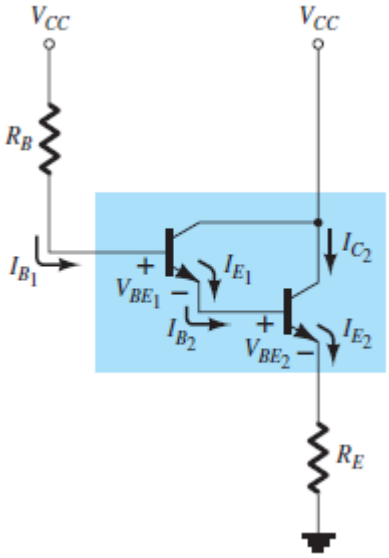


FIG. 4.66
Darlington amplifier.

For the dc analysis of Fig. 4.67 assuming a beta β_1 for the first transistor and β_2 for thesecond, the base current for the second transistor is $I_{B2} = I_{E1} = (\beta_1 + 1)I_{B1}$ and the emitter current for the second transistor is $I_{E2} = (\beta_2 + 1)I_{B2} = (\beta_2 + 1)(\beta_1 + 1)I_{B1}$



Assuming β < 1 for each transistor, we find the net beta for the configuration is

$$\beta_D = \beta_1\beta_2 \tag{4.50}$$

which compares directly with a single-stage amplifier having a gain of β_D.

Applying an analysis similar to that of Section 4.4 will result in the following equation for the base current:

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

Defining

$$V_{BE_D} = V_{BE_1} + V_{BE_2} \tag{4.51}$$

we have

$$I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E} \tag{4.52}$$

The currents

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} \tag{4.53}$$

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موضوعات المحاضرة:

Cascode configuration

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The Cascode configuration of Fig. 4.68 ties the collector of one transistor to the emitter of the other. In essence it is a voltage-divider network with a common-base configuration at the collector.

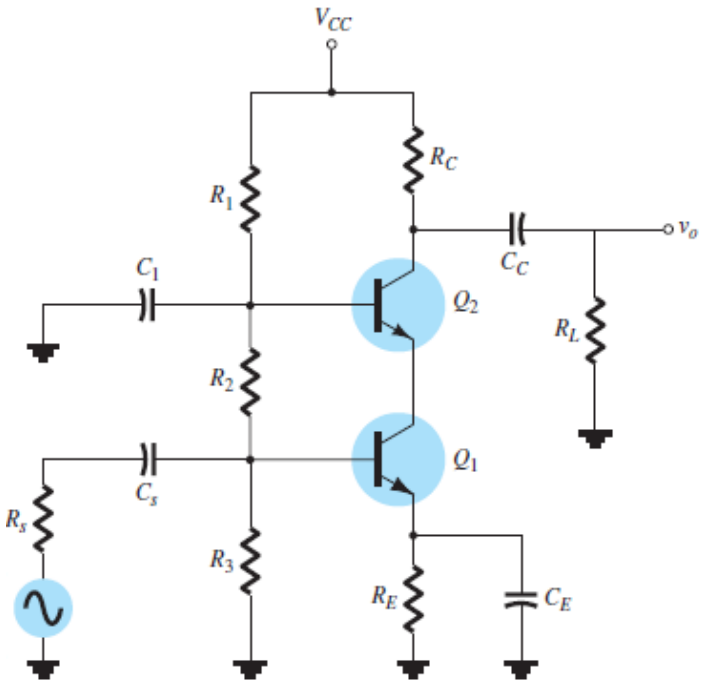

FIG. 4.68
Cascode amplifier.

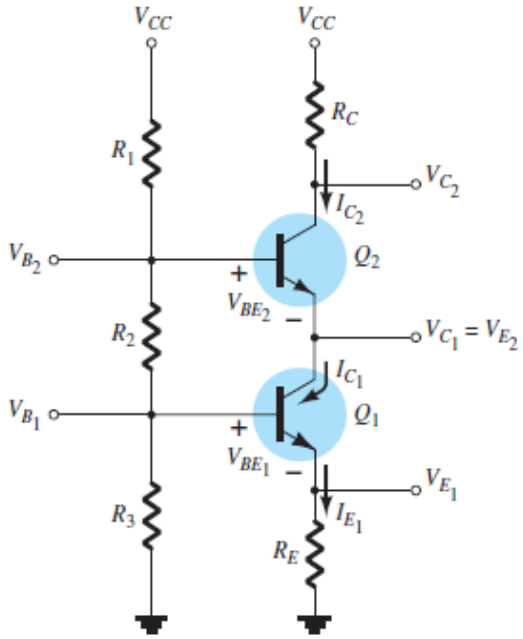

FIG. 4.69
DC equivalent of Fig. 4.68.

The dc analysis is initiated by assuming the current through the bias resistors R_1, R_2, and R_3 of Fig. 4.69 is much larger than the base current of each transistor. That is, $I_{R1} = I_{R2} = I_{R3} << I_{B1}$ or I_{B2}

The result is that the voltage at the base of the transistor Q_1 is simply determined by an application of the voltage-divider rule:

$$V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC} \qquad (4.57)$$

The voltage at the base of the transistor Q_2 is found in the same manner:

$$V_{B_2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3} V_{CC} \qquad (4.58)$$

The emitter voltages are then determined by

$$V_{E_1} = V_{B_1} - V_{BE_1} \tag{4.59}$$

and

$$V_{E_2} = V_{B_2} - V_{BE_2} \tag{4.60}$$

with the emitter and collector currents determined by:

$$I_{C_2} \cong I_{E_2} \cong I_{C_1} \cong I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_{E_1} + R_{E_2}} \tag{4.61}$$

The collector voltage V_{C_1}:

$$V_{C_1} = V_{B_2} - V_{BE_2} \tag{4.62}$$

and the collector voltage V_{C_2}:

$$V_{C_2} = V_{CC} - I_{C_2}R_C \tag{4.63}$$

The current through the biasing resistors is

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3} \tag{4.64}$$

and each base current is determined by

$$I_{B_1} = \frac{I_{C_1}}{\beta_1} \tag{4.65}$$

with

$$I_{B_2} = \frac{I_{C_2}}{\beta_2} \tag{4.66}$$

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موضوعات المحاضرة:

AC analysis of BJT transistor

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المادة العلمية:

EXAMPLE 4.26 Determine the dc levels for the currents and voltages of the direct- coupled amplifier of Fig. 4.72 . Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases where in the input impedance of the next stage is quite low. The common-collector amplifier is acting like a buffer between stages.

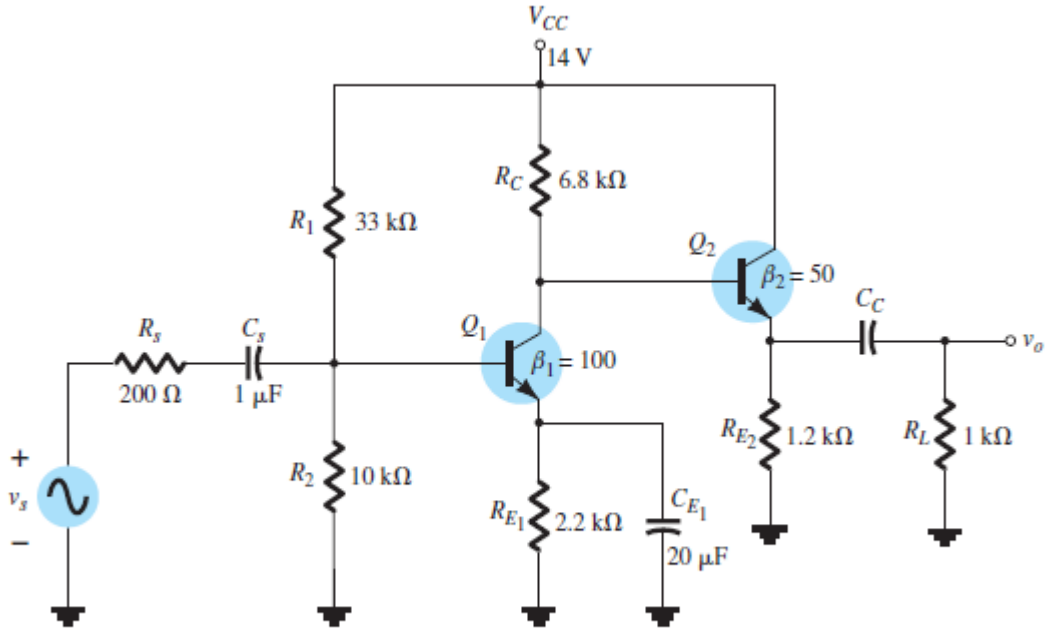

FIG. 4.72
Direct-coupled amplifier.

Solution: The dc equivalent of Fig. 4.72 appears as Fig. 4.73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 4.5.

$$I_{B_1} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_{E_1}}$$

with $$R_{\text{Th}} = R_1 \| R_2$$

and $$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

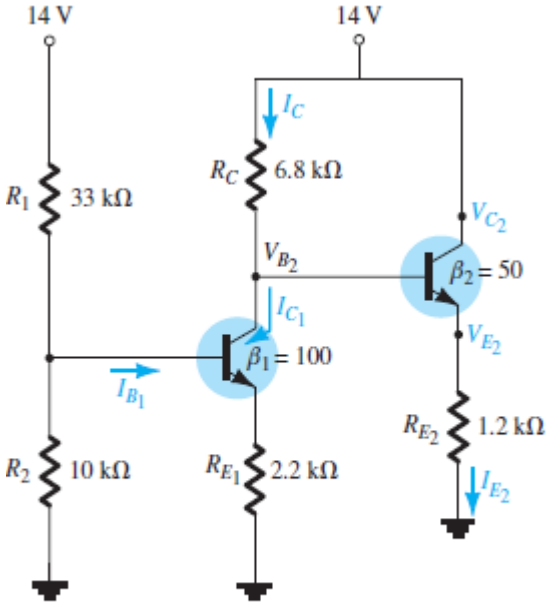

FIG. 4.73
DC equivalent of Fig. 4.72.

In this case,

$$R_{Th} = 33\,k\Omega \,\|\, 10\,k\Omega = 7.67\,k\Omega$$

and

$$E_{Th} = \frac{10\,k\Omega(14\,V)}{10\,k\Omega + 33\,k\Omega} = 3.26\,V$$

so that

$$I_{B_1} = \frac{3.26\,V - 0.7\,V}{7.67\,k\Omega + (100 + 1)\,2.2\,k\Omega}$$

$$= \frac{2.56\,V}{229.2\,k\Omega}$$

$$= \mathbf{11.17\ \mu A}$$

with

$$I_{C_1} = \beta I_{B_1}$$

$$= 100\,(11.17\,\mu A)$$

$$= \mathbf{1.12\ mA}$$

In Fig. 4.73 we find that

$$\boxed{V_{B_2} = V_{CC} - I_C R_C} \qquad \textbf{(4.76)}$$

$$= 14\,V - (1.12\,mA)(6.8\,k\Omega)$$

$$= 14\,V - 7.62\,V$$

$$= \mathbf{6.38\ V}$$

and

$$V_{E_2} = V_{B_2} - V_{BE_2}$$

$$= 6.38\,V - 0.7\,V$$

$$= \mathbf{5.68\ V}$$

resulting in

$$\boxed{I_{E_2} = \frac{V_{E_2}}{R_{E_2}}} \qquad \textbf{(4.77)}$$

$$= \frac{5.68\,V}{1.2\,k\Omega}$$

$$= \mathbf{4.73\ mA}$$

Obviously,

$$\boxed{V_{C_2} = V_{CC}} \qquad \textbf{(4.78)}$$

$$= 14\,V$$

and

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \qquad \textbf{(4.79)}$$

$$= 14\,V - 5.68\,V$$

$$= \mathbf{8.32\ V}$$

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موضوعات المحاضرة:

FET transistor characteristics

Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET),

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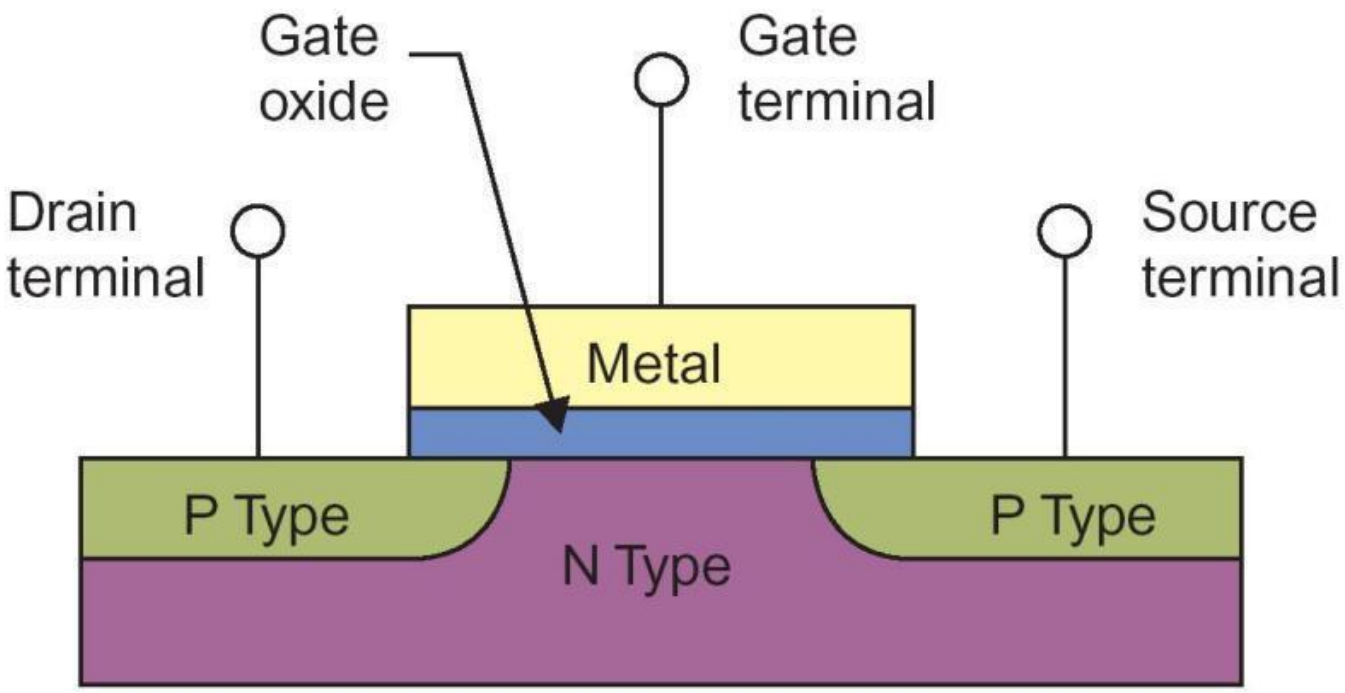

6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also
many similarities, which will be pointed out in the sections to follow.
The primary difference between the two types of transistors is the fact that:
The BJT transistor is a current-controlled device as depicted in Fig. 6.1, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

Differences:

1- FETs are voltage controlled devices. BJTs are current controlled devices.

2- FETs have a higher input impedance. BJTs have higher gains.

3- FETs are less sensitive to temperature variations and are more easily
integrated on ICs.اقلحساسًة لتغًّراتالحرارة

4- FETs are generally more static sensitive than BJTs.اكثر
حساسًة للكهرباء الساكنة

5- The FET is a unipolar device depending solely on either electron (n -channel) or hole (p -channel) conduction.

6.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

1-the JFET is a three-terminal device with one terminal capable of controlling the current between the other two
2-the major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material
3-the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material.

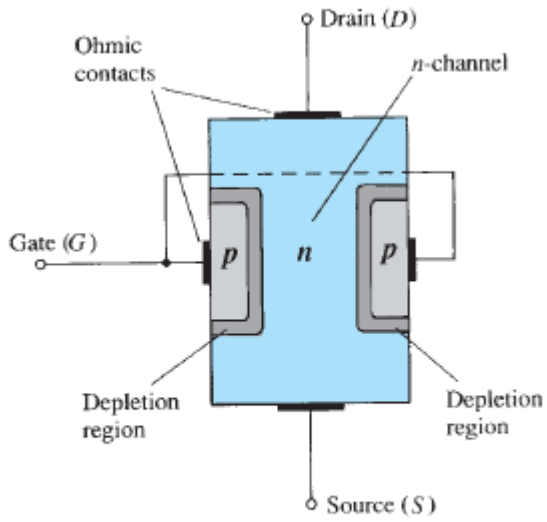

FIG. 6.3
Junction field-effect transistor (JFET).

for the JFET transistor can defined the following

1-The input circuit (gate to source) of a Jfet is reverse bias, that means the device has high input impedance 2-the drain is so biased with respect to the source , I_D flows from source to drain 3- in all Jfet $I_D=I_S$

When

V_{GS} = 0 V, VDS Some Positive Value

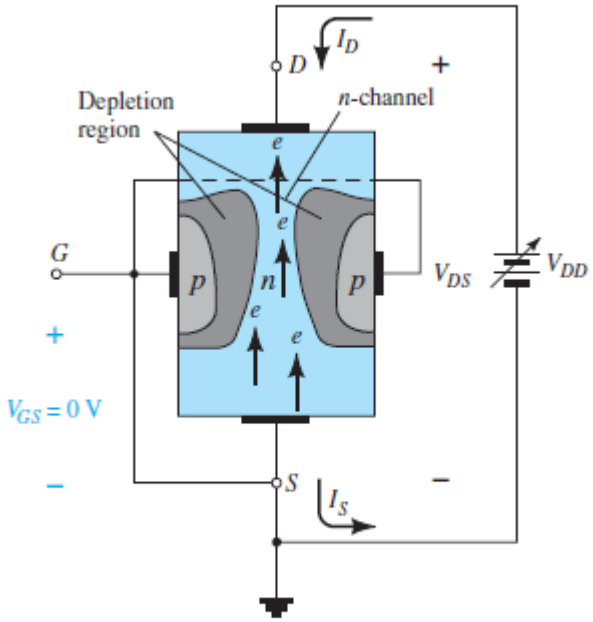

FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

The current ID will establish the voltage levels through the channel the greater the applied reverse bias in p type material , the wider is the depletion region.

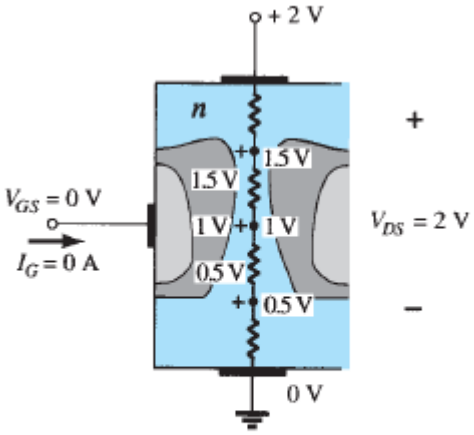

FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

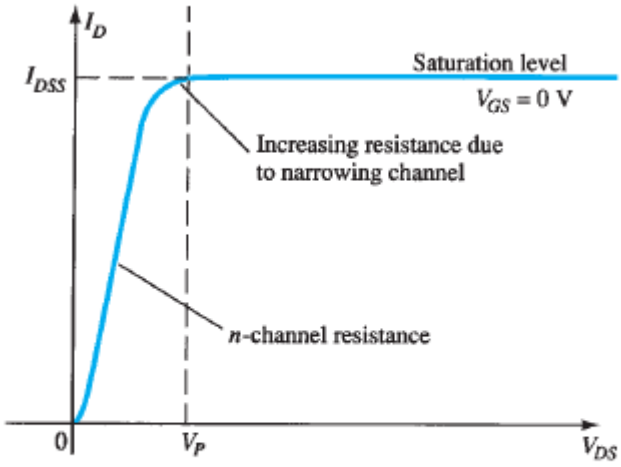

FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > V_P$.

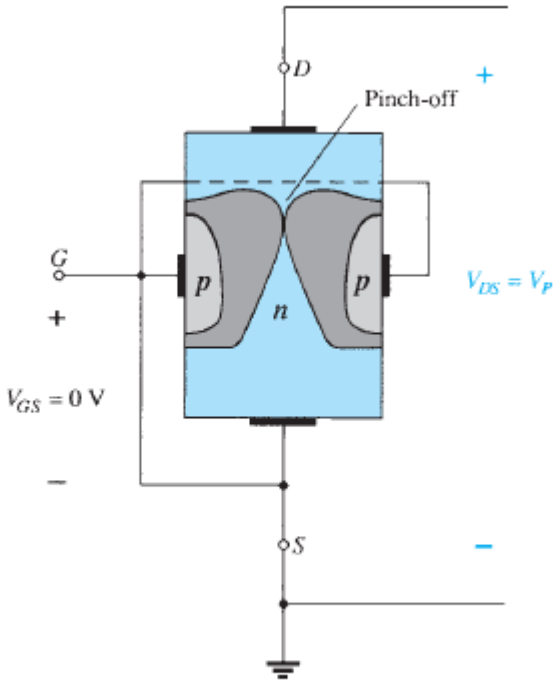

FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

When $V_{GS} < 0$ V V_{GS} is The voltage from gate to source a negative voltage is applied between G and S

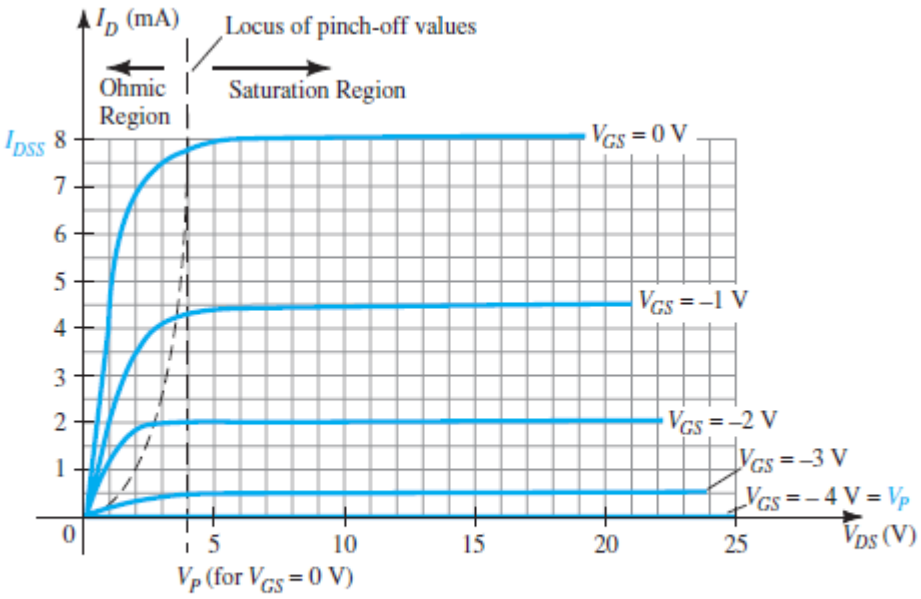

FIG. 6.11

n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative and a pinch-off voltage continues to drop as V_{GS} becomes more and more negative and the device has been "turned off." In summary: **The level of V_{GS} that results in $I_D = 0$** mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n channel devices and a positive voltage for p-channel JFETs.

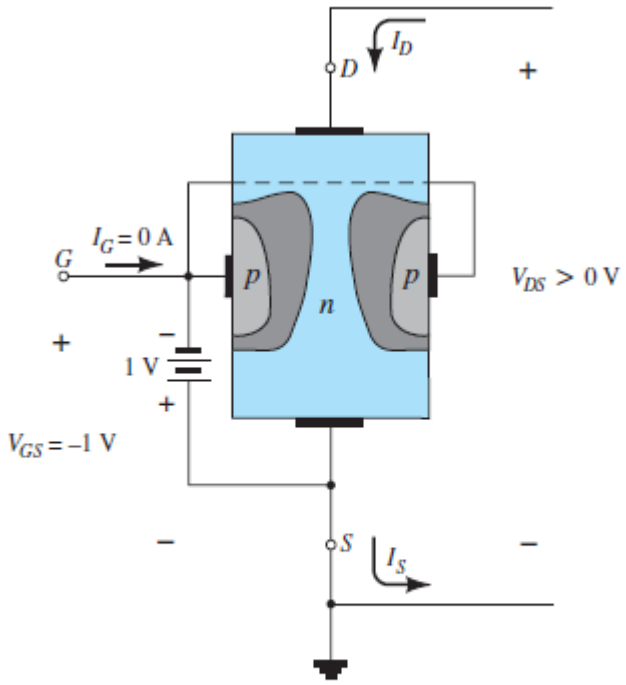

FIG. 6.10
Application of a negative voltage to the gate of a JFET.

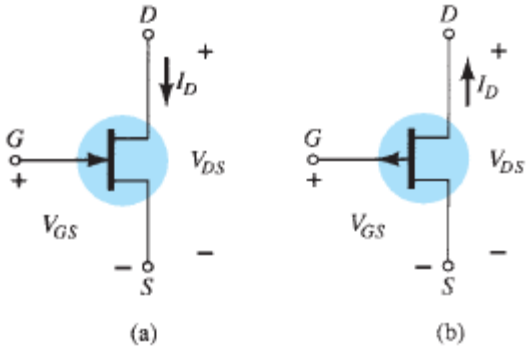

FIG. 6.14
JFET symbols: (a) n-channel; (b) p-channel.

- the n -channel device of Fig. 6.14a
- the p -channel device of Fig. 6.14b

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the ohmic or voltage-controlled resistance region. possibly for an automatic gain control system whose resistance is controlled by the applied gate-to-source voltage

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \qquad (6.1)$$

Where r_o is the resistance with $V_{GS} = 0$ V and r_d the resistance at a particular level of V_{GS}.

For an n-channel JFET with r_o equal to 10 k· ($V_{GS} = 0$ V, $V_P = 6$ V), Eq. (5.1) will result in 40 k· at $V_{GS} = 3$ V.

p -Channel Devices

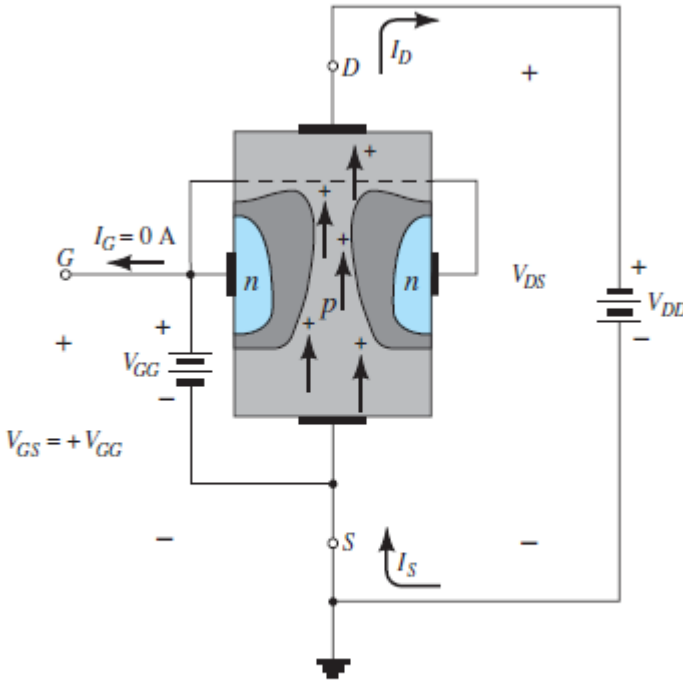

FIG. 6.12
p-Channel JFET.

The defined current directions are reversed

Applied voltage is positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS}

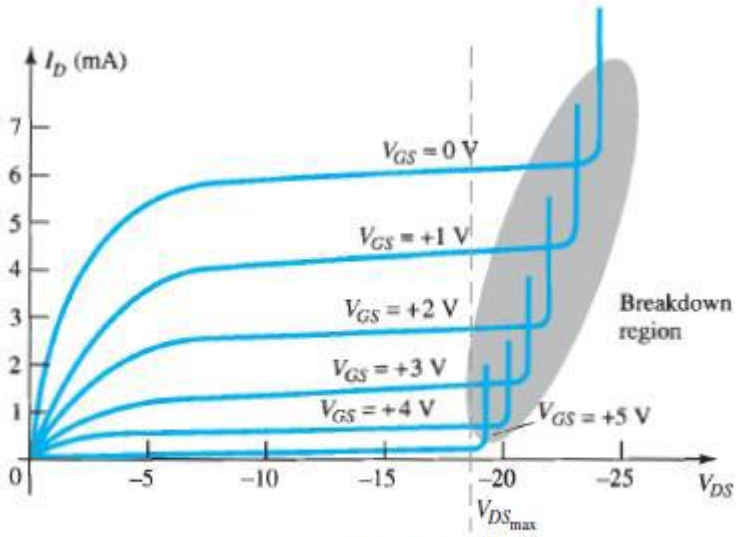

FIG. 6.13

p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

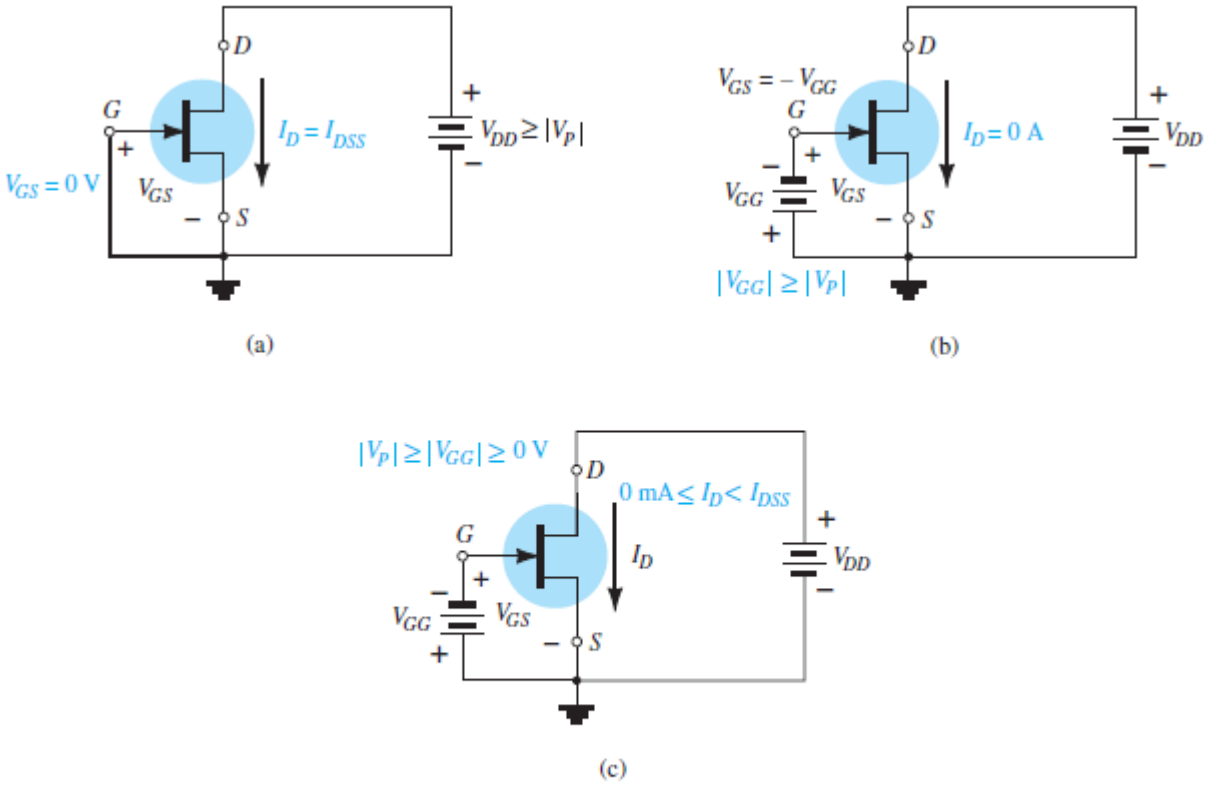

FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

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موضوعات المحاضرة:

TRANSFER CHARACTERISTICS

الأساليب والأنشطة والوسائل التعليمية

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المادة العلمية:

6.2 TRANSFER CHARACTERISTICS

The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (5.3)$$

control variable

constants

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 6.11 . In Fig. 6.17 two graphs are provided

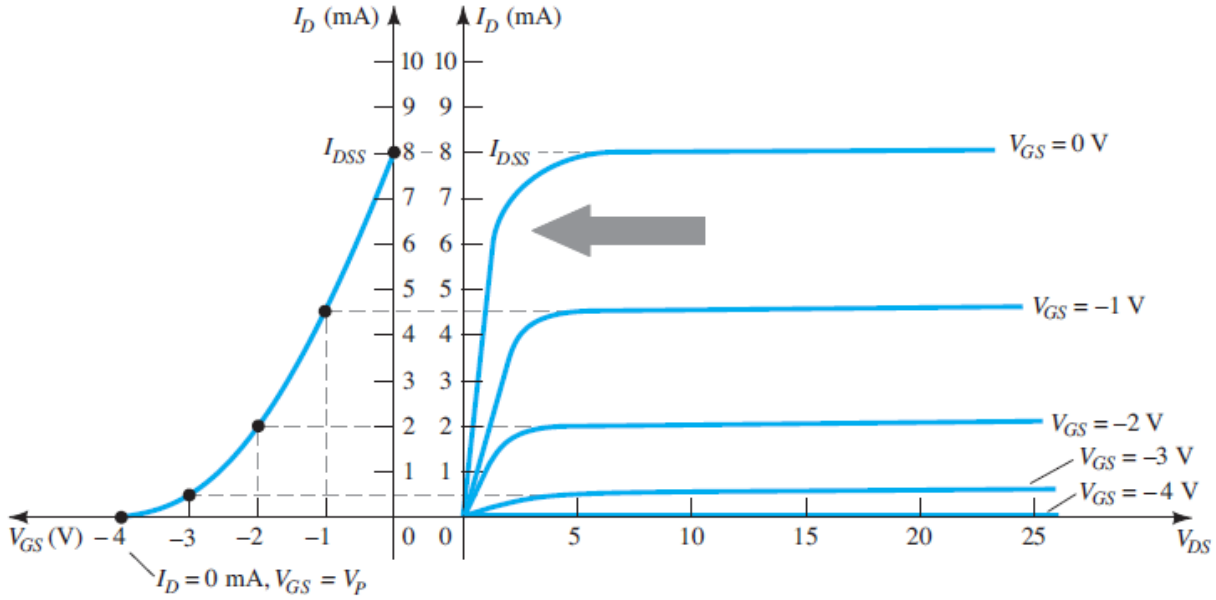

FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

In review:

$$\boxed{\text{When } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS}} \tag{6.4}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0 \text{ mA}} \tag{6.5}$$

Applying Shockley's Equation

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (6.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}\,|_{V_{GS}=0\text{ V}}} \tag{6.6}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$

$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0\text{ A}\,|_{V_{GS}=V_P}} \tag{6.7}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}\,(0.75)^2$$

$$= 8\text{ mA}\,(0.5625)$$

$$= \mathbf{4.5\text{ mA}}$$

By using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in equation (6.8)

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \tag{6.8}$$

Let us test Eq. (6.8) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$\begin{aligned} V_{GS} &= -4\text{ V}\left(1 - \sqrt{\frac{4.5\text{ mA}}{8\text{ mA}}}\right) \\ &= -4\text{ V}(1 - \sqrt{0.5625}) = -4\text{ V}(1 - 0.75) \\ &= -4\text{ V}(0.25) \\ &= \mathbf{-1\text{ V}} \end{aligned}$$

as substituted in the above calculation and verified by Fig. 6.17.

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موضوعات المحاضرة:

Shorthand method

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الأساليب والأنشطة والوسائل التعليمية

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Shorthand Method

If we specify $\mathbf{V}_{GS}$ to be one-half the pinch-off value $\mathbf{V}_P$, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$

$$= I_{DSS}(0.25)$$

and

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}} \qquad \textbf{(6.9)}$$

The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and

$$V_{GS} \cong 0.3V_P|_{I_D=I_{DSS}/2} \qquad \textbf{(6.10)}$$

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\ mA} \quad \text{and} \quad V_{GS} = \mathbf{0\ V}$$

and

$$I_D = \mathbf{0\ mA} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\ V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\ mA}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\ V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

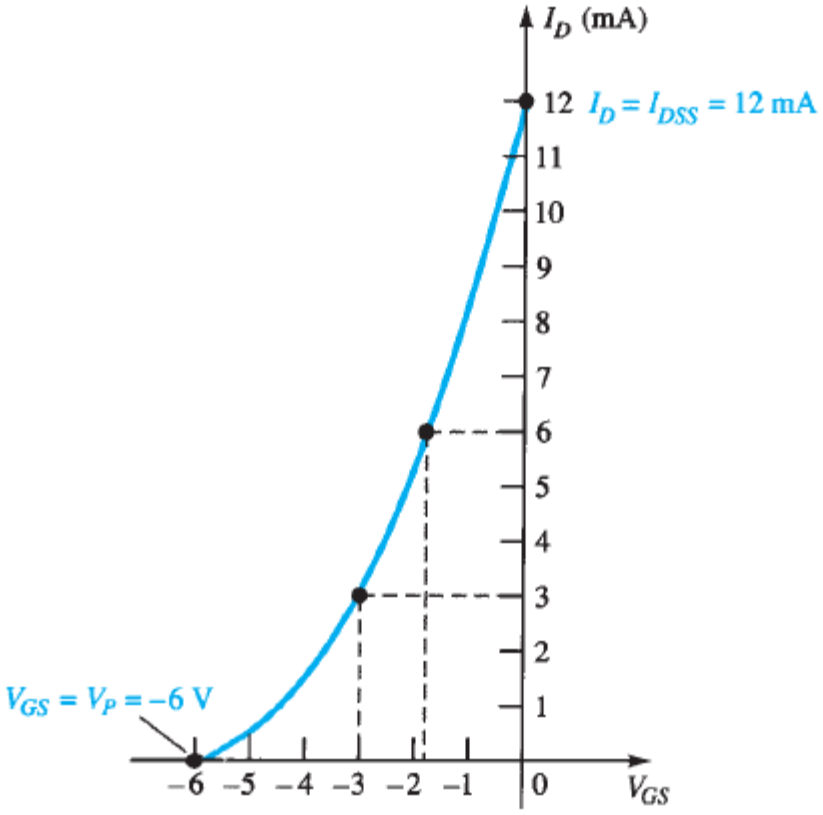

FIG. 6.18
Transfer curve for Example 6.1.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

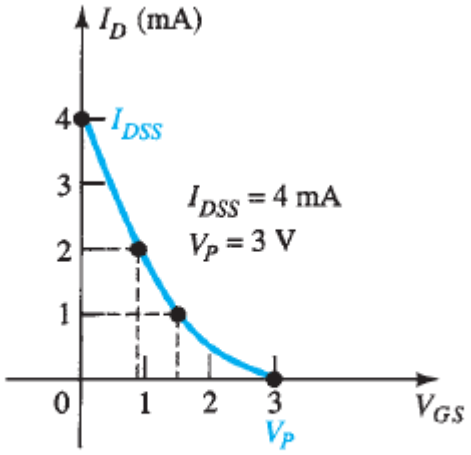

FIG. 6.19

Transfer curve for the p-channel device of Example 6.

6.٣ DEPLETION-TYPE MOSFET

The name MOSFET stands for metal–oxide–semiconductor field -effect transistor

Basic Construction

1-A slab of p -type material is formed from a silicon base and is referred to as the substrate.

2- In some cases the substrate is internally connected to the source terminal

3-The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel as shown in the figure

4-The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a dielectric

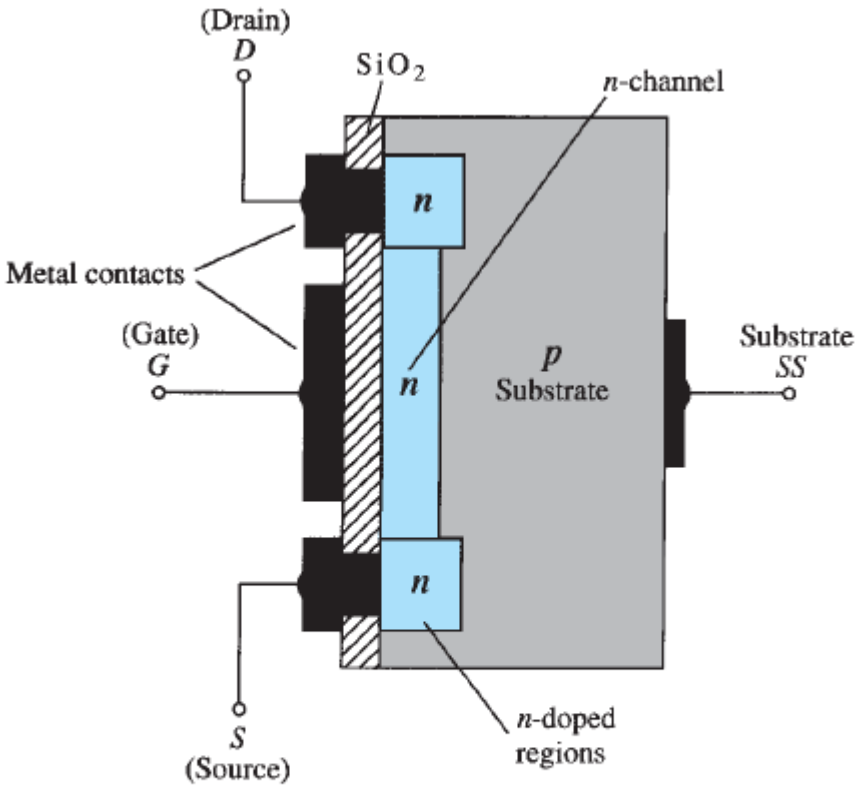

FIG. 6.24
n-Channel depletion-type MOSFET.

In Fig. 6.27, V_{GS} is set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the magnitude of the negative bias established by V_{GS}, The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}

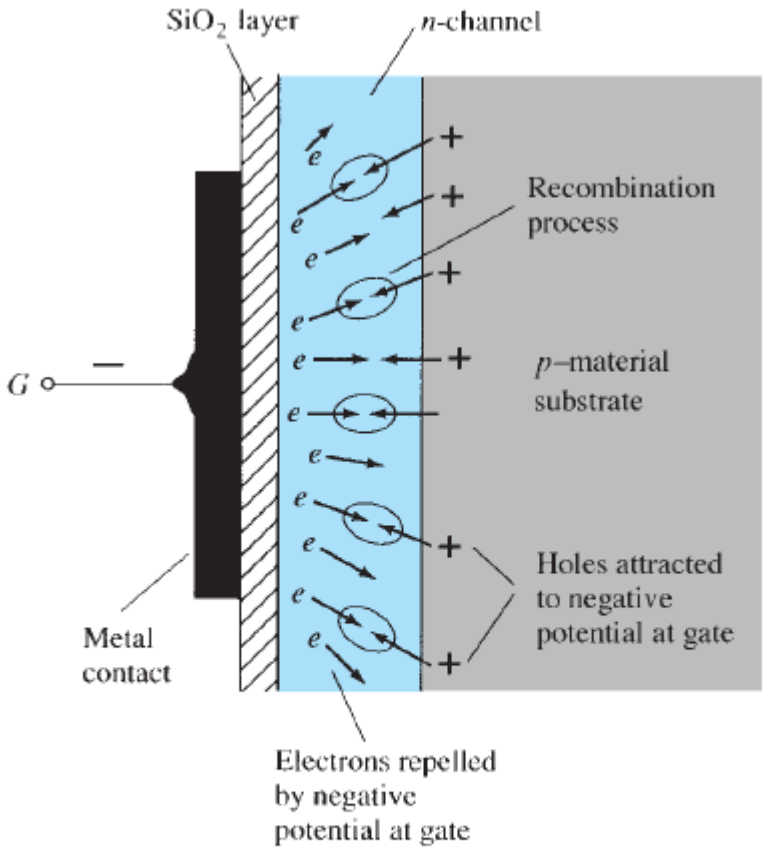

FIG. 6.27
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

In Fig. 6.26 for VGS = -1 V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET. **For positive values of V_{GS}** , the positive gate will draw additional electrons (free carriers) from the p -type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles As the gate- to-source voltage continues to increase in the positive direction, Fig. 6.26 reveals that the drain current will increase

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موضوعات المحاضرة:

FET transistor characteristics and applications

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6.٤ ENHANCEMENT-TYPE MOSFET

Basic Construction

1-p -type material is formed from a silicon base and is again referred to as the substrate
2-the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.
3-The drain current is now cut off until the gate-to-source voltage reaches a specific magnitude.

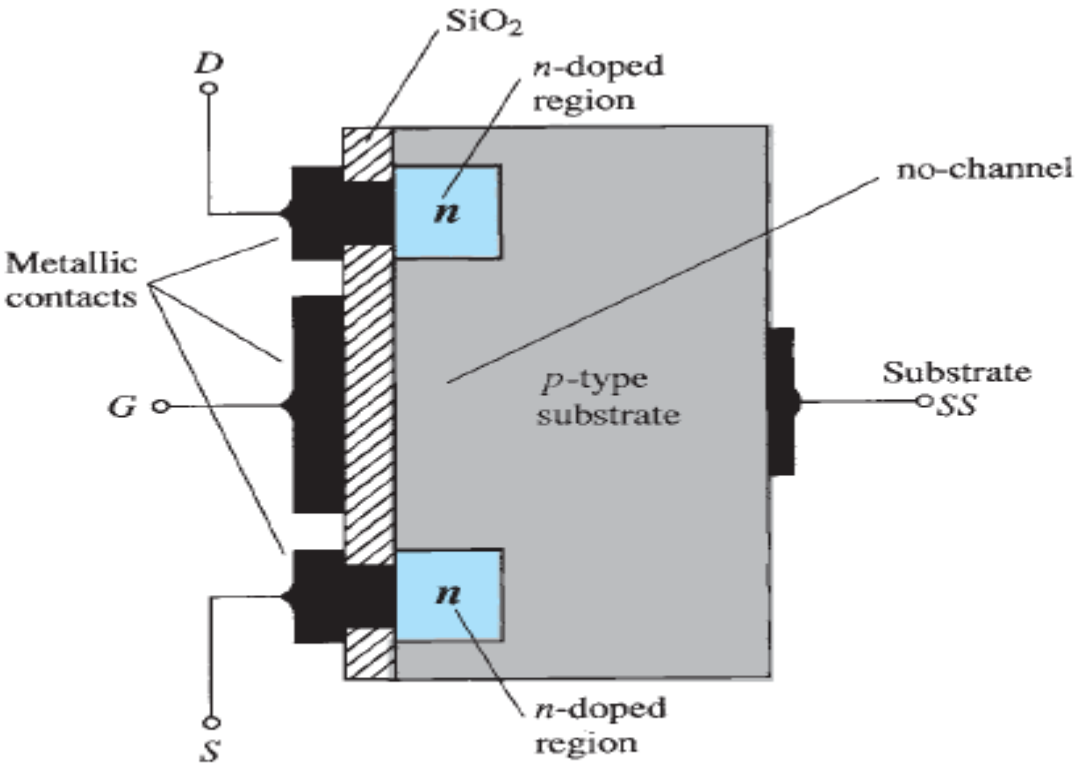

FIG. 6.32
n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

1- If V_{GS} is set at 0V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0A

2-In Fig.6.33, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0V, establishing the drain and the gate at a positive potential with respect to the source

3-The positive potential at the gate will pressure the holes (since like charges repel) in the p -substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p -substrate, as shown in the figure. The result is a depletion region near the SiO2 insulating layer void of holes. However, the electrons in the p -substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer.

4- with VGS increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n -type region can support a measurable flow between drain and source

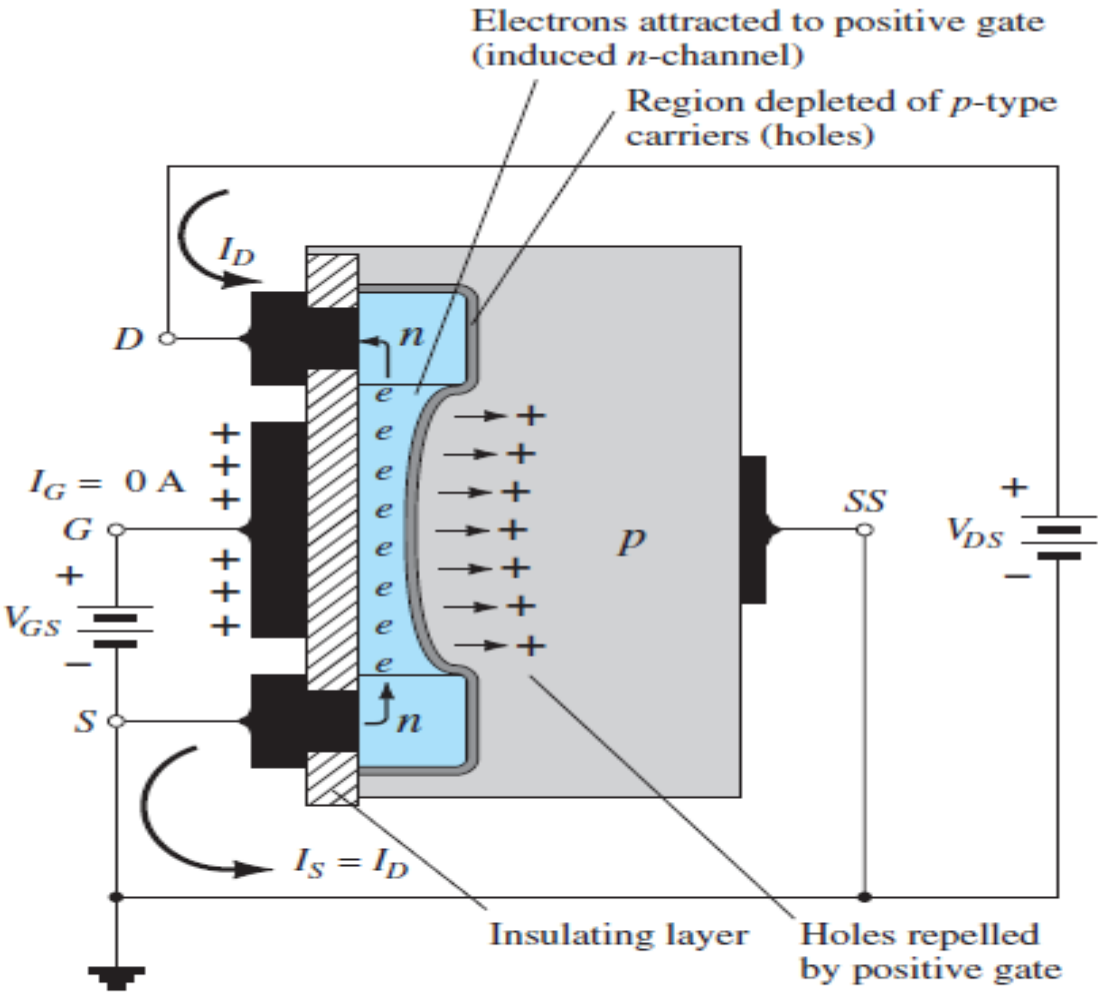

FIG. 6.33

Channel formation in the n-channel enhancement-type MOSFET.

$$V_{DG} = V_{DS} - V_{GS} \qquad (6.13)$$

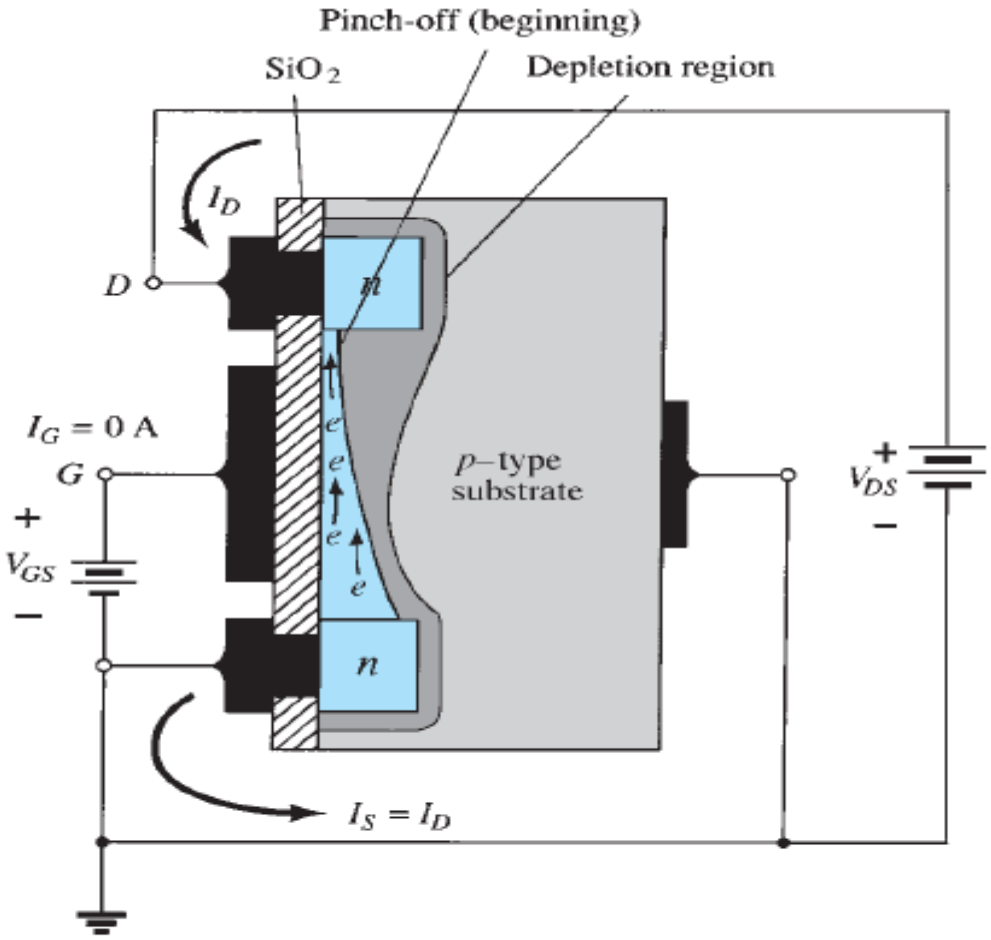

FIG. 6.34

Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{sat}} = V_{GS} - V_T \qquad \textbf{(6.14)}$$

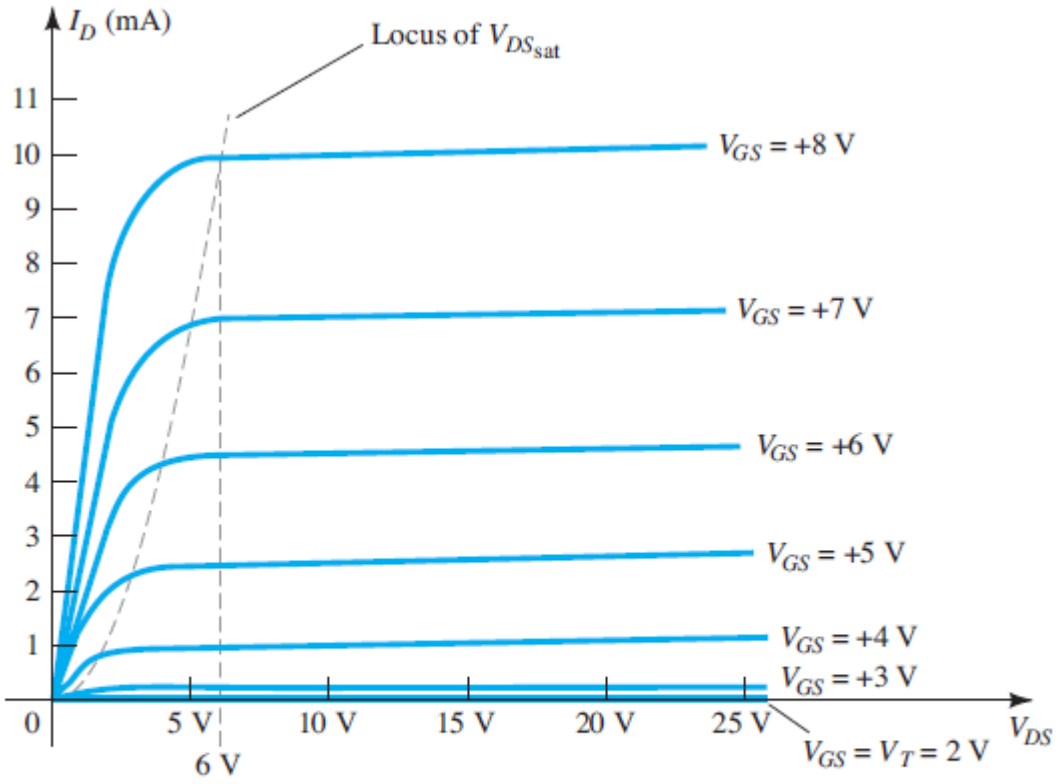

FIG. 6.35

Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ *V and* $k = 0.278 \times 10^{-3}$ A/V^2.

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موضوعات المحاضرة:

Frequency response

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المادة العلمية:

FET BIASING

$$I_G \cong 0\ \text{A} \qquad (7.1)$$

and

$$I_D = I_S \qquad (7.2)$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (7.3)$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \qquad (7.4)$$

1

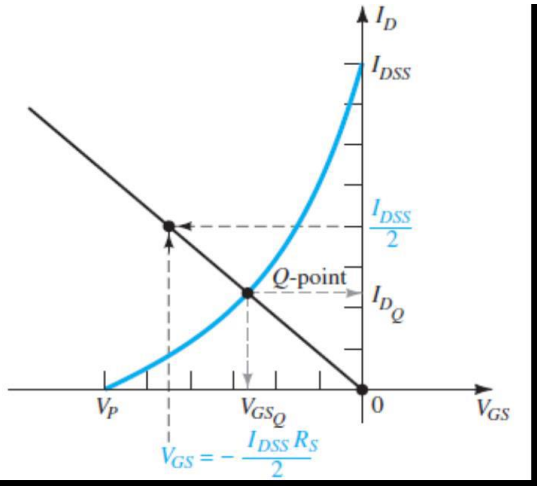

FIG. 7.11

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS}R_S}{2}$$

The level of V DS can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but $$I_D = I_S$$

and $$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad (7.11)$$

In addition,

$$V_S = I_D R_S \quad (7.12)$$

$$V_G = 0\,\text{V} \quad (7.13)$$

and $$V_D = V_{DS} + V_S = V_{DD} - V_{R_D} \quad (7.14)$$

FOR Draw the transfer curve we are using next schedule

VGS	ID
VGS = 0.3 VP	ID = 1/2 IDSS
VGS = 1/2 VP	ID = 1/4 IDSS
VGS = VP	ID = 0
VGS = 0	ID = IDSS

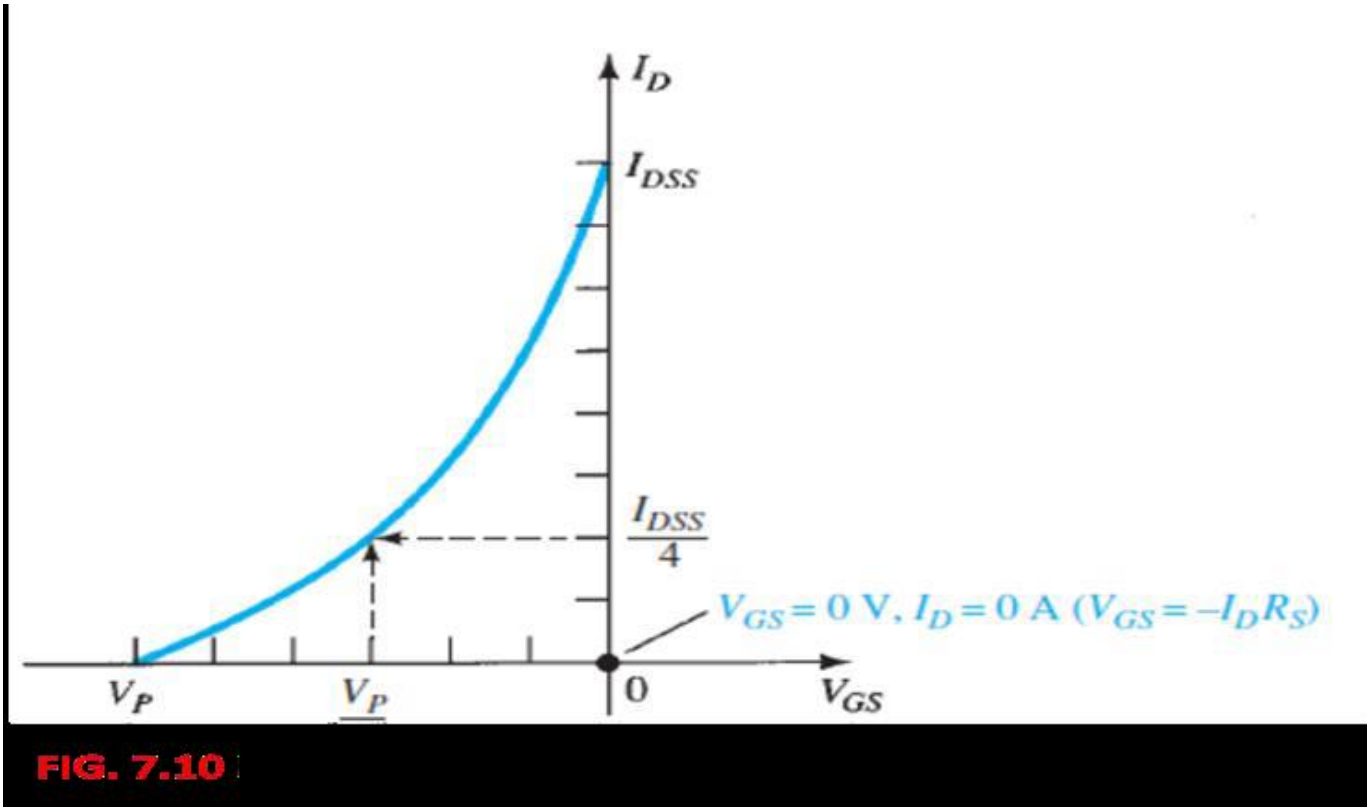

FIG. 7.10

The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 7.10 one point on the straight line is defined by ID = 0 A and VGS = 0 V

The second point for Eq. (7.10) requires that a level of VGS or ID be chosen and the corresponding level of the other quantity be determined using Eq.

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موضوعات المحاضرة:

II Frequency response

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EXAMPLE 7.7 Repeat Example 7.6 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

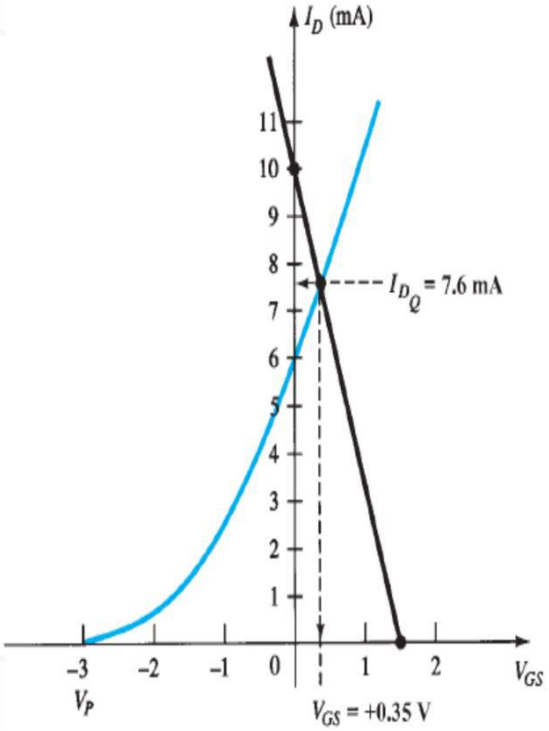
$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$



The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

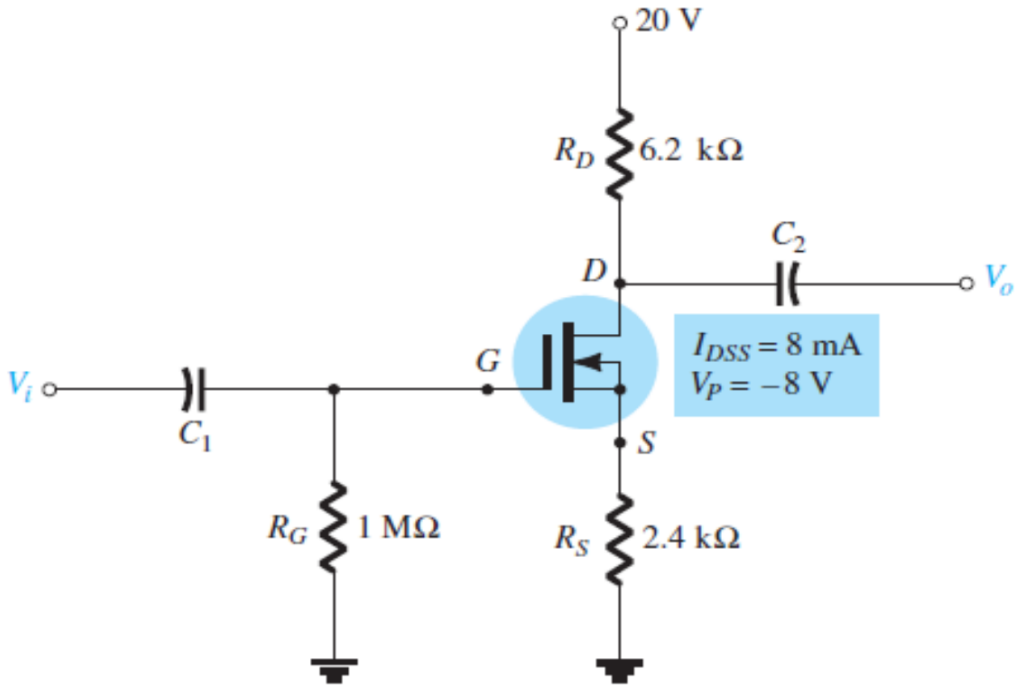
$$I_{D_Q} = \mathbf{7.6\text{ mA}}$$
$$V_{GS_Q} = \mathbf{+0.35\text{ V}}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega)$$
$$= \mathbf{3.18\text{ V}}$$

EXAMPLE 7.8 Determine the following for the network of Fig. 7.33:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.



Feedback Biasing Arrangement

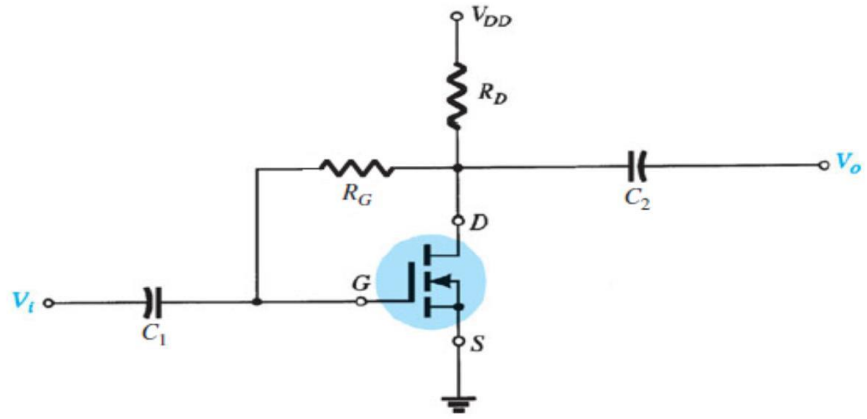


FIG. 7.37
Feedback biasing arrangement.

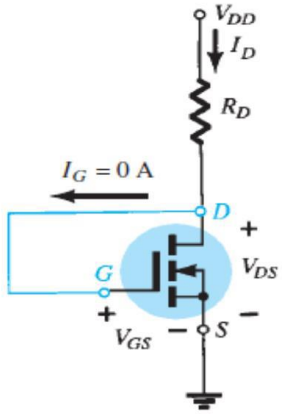


FIG. 7.38
DC equivalent of the network of Fig. 7.37.

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الوحدة السادسة - المحاضرة الرابعة والعشرون - الزمن: 120 دقيقة

موضوعات المحاضرة:

Operational Amplifiers and their applications

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

OP-AMP and its applications
Introduction
- The operational amplifier (Op-Amp) concept was introduced by Tellegen in 1954 under the
name of “ideal amplifier”. The first Op-Amps with discrete transistors appeared in production
in 1956. One of the first analog ICs was an Op-Amp developed by R. Widlar in 1964. The operational amplifier is still the integrated circuit with highest production volume.
- OP-AMP is a very high-gain directly-coupled negative-feedback amplifier which can amplify
signals having frequency ranging from 0 Hz to 1 MHz.
- OP-AMP is so named because it was originally designed to perform mathematical operations
like summation, subtraction, multiplication, differentiation integration ...etc. Present day usage
is much wider in scope but the popular name OP-AMP continues.
nd in analog computers applications.
- Typical applications of OP-AMP are scale changing, analog computer operations, in instrumentation and control systems and a great variety of phase-shift and oscillator

circuits.
- Example of OP-AMPs [LM 108, LM 208, 741,....]
OP-AMP Circuit and Symbol
Standard triangular symbol of an OP-AMP is shown in Fig.1. All OP-AMPs have a minimum of five terminals:
1. inverting input terminal (labeled with a minus sign),
2. non-inverting input terminal (labeled with a plus sign),
3. output terminal,
4. positive bias supply terminal,
5. negative bias supply terminal.

- When an OP-AMP is operated without connecting any resistor or capacitor from its output to
any one of its inputs (i.e., without feedback), it is said to be in the open-loop condition. The
specifications of OP-AMP under such condition are called open-loop specifications and exhibiting the open-loop voltage gain (AOL).
- An op amp amplifies the difference between two input signals v1&v2; i.e amplifies (vd), where
(vd=v1-v2)
vo= AOL*vd (AOL for actual op amp is extremely high i.e., about 106)
However, if (vd=1 V), it does not mean that will be amplified to 106 V at the output. Actually, the maximum value of vo is limited by the basis supply voltage and is called its saturation voltage. This voltage is approximately 2V smaller than the power-supply voltage
(VCC). In other words, the amplifier is linear over the range
$-(VCC - 2) < vo < VCC - 2$, typically ± 15 V.
Example1: An op amp has saturation voltage Vsat =10 V, an open-loop voltage gain of -105,
and input resistance of 100k. Find (a) the value of vd that will just drive the amplifier to saturation and (b) the op amp input current at the starting of saturation.

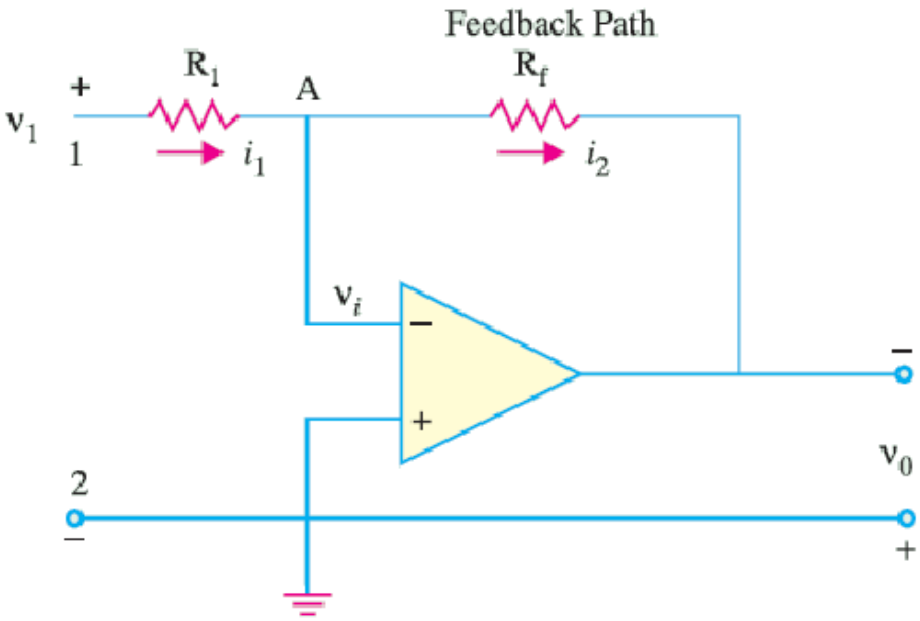

Fig. 2

Ideal Operational Amplifier

An ideal OP-AMP has the following characteristics :

1. its open-loop gain AOL is infinite i.e., Aν = − ∞
2. its input resistance Ri (measured between inverting and non-inverting terminals) is infinite

i.e., Ri = ∞ Ω. This means that the input current i = 0.

3. its output resistance R0 (seen looking back into output terminals) is zero i.e., R0 = 0 Ω. This

means that v0 is not dependent on the load resistance connected across the output.

4. it has infinite bandwith i.e., it has flat frequency response from dc to infinity.

Virtual Ground and Summing Point

Fig. 2 shows an OP-AMP which employs negative feedback with the help of resistor Rf which

feeds a portion of the output to the input. The concept of virtual ground arises from the fact that

input voltage vi at the inverting terminal of the OP-AMP is forced to a small value (assumed

zero). Hence, point A is essentially at ground voltage and is referred to as virtual ground. Obviously, it is not the actual ground.

When v1 is applied, point A attains some positive potential and at the same time v0 is brought

into existence. Due to negative feedback, some fraction of the output voltage is fed back to point A antiphase with the voltage already existing there (due to v1). The algebraic sum of the two voltages is almost zero so that vi ≅ 0. Obviously, vi will become exactly zero when negative feedback voltage at A is exactly equal to the positive voltage produced by

v1 at A.
Another point worth considering is that there exists a virtual short between the two terminals of the OP-AMP because vi = 0. It is virtual because no current flows (remember i = 0) despite the existence of this short.

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اهداف المحاضرة:

يفهم الطالب ماهي ال ***Operational Amplifiers and their applications***
وماهو ال Inverting Amplifier

موضوعات المحاضرة:

Operational Amplifiers and their applications
Inverting Amplifier

الأساليب والأنشطة والوسائل التعليمية

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المادة العلمية:

OP-AMP Applications

1- Inverting Amplifier

The inverting amplifier of Fig. 3 has its noninverting input connected to ground. A signal (vin)
is applied through input resistor R1, and negative current feedback is implemented through
feedback resistor Rf . Output voltage (vo) has polarity opposite that of input.

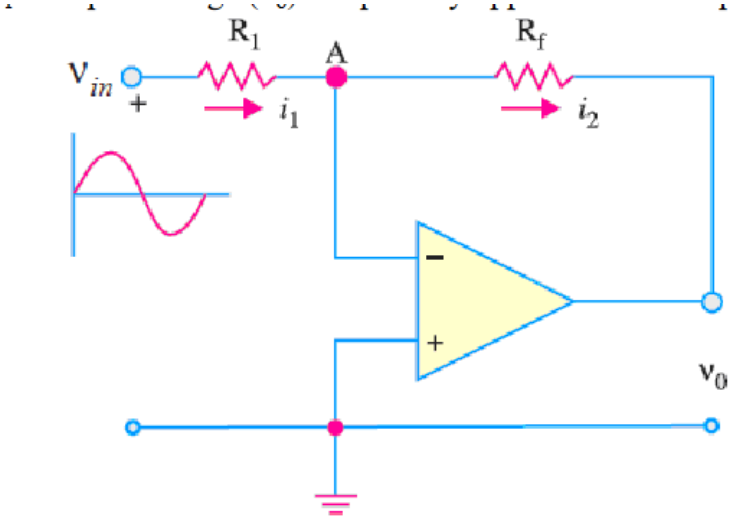


Fig. 3

The gain of the inverting amplifier can be driven as follow:
Since point A is at ground potential (VA=0) and iin=0,

Fig. 3

The gain of the inverting amplifier can be driven as follow:
Since point *A* is at ground potential (V_A=0) and i_{in}=0,

i1=i2 ➔ $i_1 = \frac{v_{in} - v_A}{R_1}$ and $i_2 = \frac{v_A - v_0}{R_f}$

$$\frac{v_{in} - 0}{R_1} = \frac{0 - v_0}{R_f} \rightarrow \frac{v_0}{R_f} = -\frac{v_{in}}{R_1} \quad \text{or} \quad \frac{v_0}{v_{in}} = -\frac{R_f}{R_1}$$

$$A_v = -\frac{R_f}{R_1} \quad \text{Also, } v_0 = -A_v v_{in}$$

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors *R*1 and *Rf* and is independent of the amplifier parameters.

2- Noninverting Amplifier

The noninverting amplifier of Fig. 4 is realized by grounding R1 of Fig. 3 and applying the input signal at the noninverting. Here, polarity of v0 is the same as that vin.

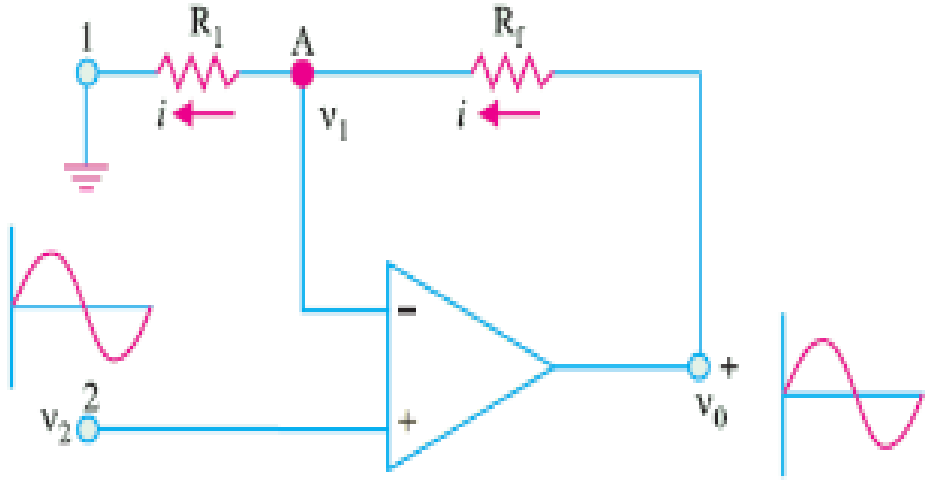


Fig. 4

The gain of the noninverting amplifier can be driven as follow:
Because of virtual short between the two OP-AMP terminals, voltage across R1 is the input voltage vin. Also, v0 is applied across the series combination of R1 and Rf.

$$\therefore v_{in} = iR_1 \quad , v_0 = i(R_1 + R_f)$$

$$A_v = \frac{v_0}{v_{in}} = \frac{i(R_1 + R_f)}{iR_1} \quad \text{or} \quad A_v = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

3- Voltage Follower

It provides a gain of unity without any phase reversal. This circuit (Fig. 5) is useful as a buffer or isolation amplifier because it allows, input voltage *vin* to be transferred as output voltage v0 while at the same time preventing load resistance *RL* from loading down the input source. It is due to the fact that its $Ri = \infty$ and $R0 = 0$.

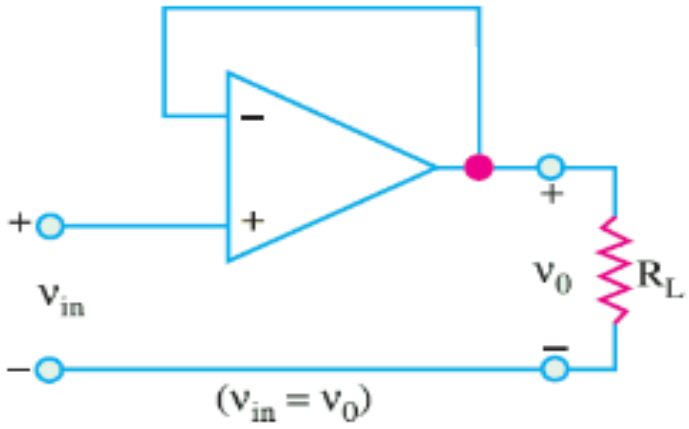
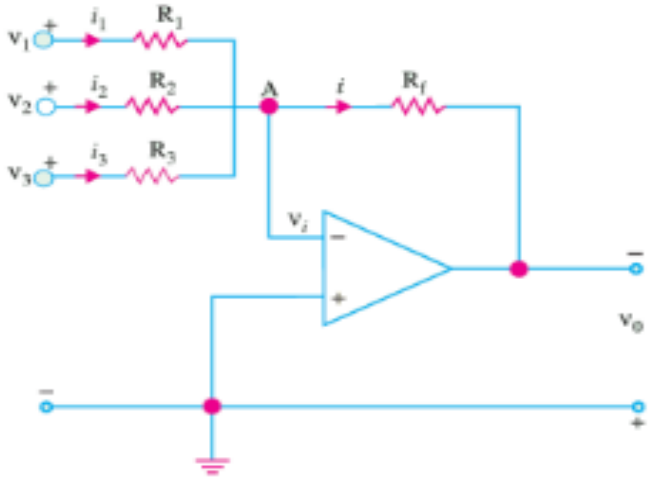


Fig. 5

4- Adder or Summer Amplifier

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. It is basically similar to a Fig. 3 except that it has more than one input. Fig. 6 shows a three-input inverting adder circuit. As seen, ***the output voltage is phase-inverted.***



Calculations

As before, we will treat point *A* as virtual ground

$$i_1 = \frac{v_1}{R_1} \quad , \quad i_2 = \frac{v_2}{R_2} \quad , \quad i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_0}{R_f}$$

Applying *KCI* to point *A*, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or $$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_0}{R_f}\right) = 0$$

$$\therefore \quad v_0 = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$

If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R} (v_1 + v_2 + v_3)$$

If $R_f = R$, then ouput exactly equals the sum of inputs.

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اهداف المحاضرة:

يفهم الطالب ماهي ال ***Operational Amplifiers and their applications***
وماهو ال ***Subtractor***

موضوعات المحاضرة:

Operational Amplifiers and their applications
Subtractor

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

5- Subtractor

The function of a subtractor is to provide an output proportional to the difference of two input signals. As shown in Fig. 7. The inputs are applying at the inverting and noninverting terminals.

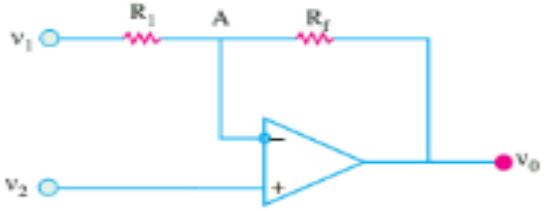

Fig. 7

Calculations

According to Superposition theorem;
v0 = v0′ + v0″
where v0′ is the output produced by v1 and v0″ is that produced by v2.

Now $v_0' = -\frac{R_f}{R_1} \cdot v_1$ (see inverting amplifier equation)

$v_0'' = \left(1+\frac{R_f}{R_1}\right) v_2$ (see noninverting amplifier equation)

If $Rf >> R1$ and $Rf/R1 >> 1$, hence

$$v_0 \equiv \frac{R_f}{R_1}(v_2 - v_1)$$

Further, If $Rf = R1$, then
v0 = (v2 − v1) = difference of the two input voltages

Example: Find the output voltages of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, Rf = 1 MΩ.
v1 = −3 V, v2 = + 3V, v3 = + 2V; R1 = 250 KΩ, R2 = 500 KΩ, R3 = 1 M Ω (ans. Vo=4v)

Example: In the subtractor circuit, R1 = 5 K, Rf = 10 K, v1 = 4 V and v2 = 5V. Find the value of output voltage.

Solution:

$$v_0 = \left(1+\frac{R_f}{R_1}\right)v_1 - \frac{R_f}{R_1}v_2 = \left(1+\frac{10}{5}\right)4 - \frac{10}{5}\times 5 = +\,2V$$

Example: Design an OP-AMP circuit that will produce an output equal to − (4 v1 + v2 +0·1v3). Write an expression for the output and sketch its output waveform when v1 = 2 sin ωt, v2 =+5V dc and v3 = −100 Vdc.

Solution:

$$v_0 = -\left[\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right] \quad ...(1)$$

$$v_0 = -(4\,v_1 + v_2 + 0{\cdot}1\,v_3) \quad ...(2)$$

Comparing equations **(1)** and **(2)**, we find,

$$\frac{R_f}{R_1} = 4, \quad \frac{R_f}{R_2} = 1, \quad \frac{R_f}{R_3} = 0{\cdot}1$$

Therefore if we assume $Rf = 100\ K$, then $R1 = 25\ K$, $R2 = 100\ K$ and $R3 = 10\ K$. With there values of $R1$, $R2$ and $R3$, the *OP-AMP* circuit is as shown in Fig. 8 (*a*).

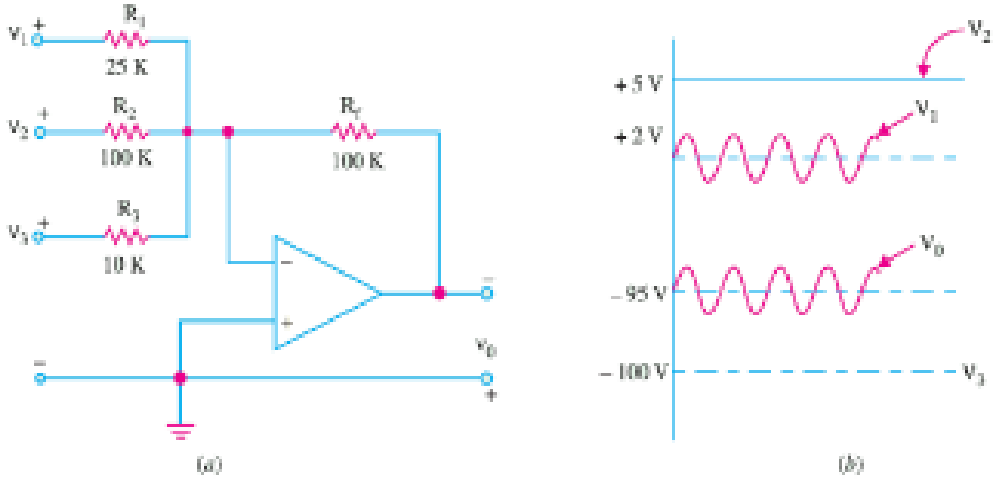

Fig. 8

With the given values of v1 = 2 sin ωt, v2 = + 5V, v3 = − 100 V dc, the output voltage, v0 = 2sin ωt+ 5 − 100 = 2 sin ωt − 95 V. The waveform of the output voltage is sketched as shown in Fig.8 (*b*).

6- Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage. A simple example of integration is shown in Fig. 9, where input is dc level and its integral is *a linearly-increasing ramp output*. The actual integration circuit is similar to the inverting circuit except that **the feedback component is a capacitor C instead of a resistor Rf**.

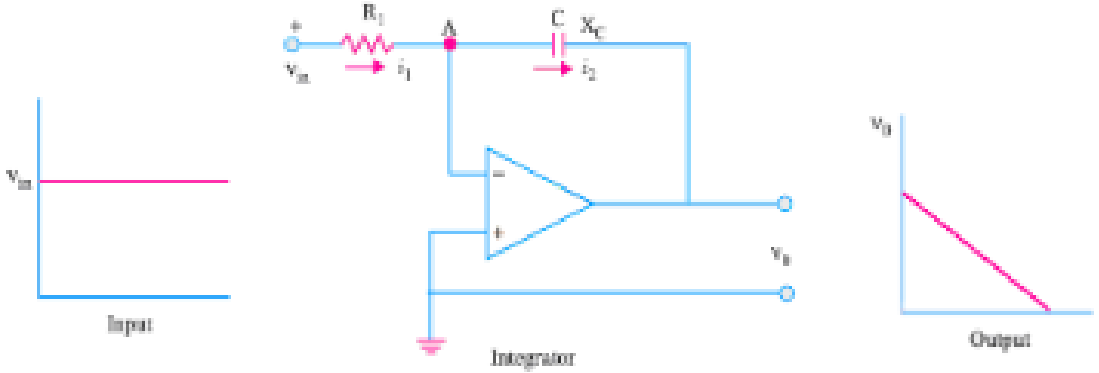

Fig. 9

Calculations

As before, If the op amp is ideal, point *A* will be treated as virtual ground, and v_{in} appears across R_1. Thus

$$i_1 = \frac{v_{in}}{R_1}$$

$$i_1 = i_c = C\frac{dv_c}{dt} = -C\frac{dv_o}{dt} \quad (\text{since } v_i = -v_o)$$

But, with negligible current into the op amp, the current through R1 = current flow through C. Then

$$\frac{v_{in}}{R_1} = -C\frac{dv_o}{dt} \rightarrow dv_o = -\frac{1}{R_1 C}v_{in}dt \rightarrow v_o = -\frac{1}{R_1 C}\int v_{in}dt$$

It is seen from above that output (left-hand side) is an integral of the input, with an inversion and a scale factor of $1/CR_1$. This ability to integrate a given signal enables an analog computer solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operation.

Note: we can integrate more than one input as shown below in Fig. 10. With multiple inputs, the output is given by

$$v_0(t) = -\left[K_1\int v_1(t)\,dt + K_2\int v_2(t)\,dt + k_3\int v_3(t)\,dt\right]$$

where $K_1 = \frac{1}{CR_1}$, $K_2 = \frac{1}{CR_2}$ and $K_3 = \frac{1}{CR_3}$

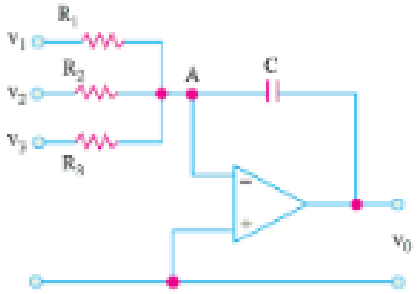

Fig. 10

Example: A 5mV, 1-kHz sinusoidal signal is applied to the input of an OP-AMP integrator, for which R = 100 K and C = 1 μF. Find the output voltage.

Solution:

$$-\frac{1}{CR} = \frac{1}{10^5 \times 10^{-6}} = -10$$

The equation for the sinusoidal voltage is

$$v_1 = 5\sin 2\pi f t = 5\sin 2000\,\pi t$$

Obviously, it has been assumed that at $t = 0$, $v_1 = 0$

$$v_0(t) = -10\int_0^t 5\sin 2000\,\pi t = -50\left|\frac{-\cos 2000\,\pi t}{2000}\right|_0^t$$

$$= -\frac{1}{40\,\pi}(\cos 2000\,\pi t - 1)$$

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اهداف المحاضرة:

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Differentiato

موضوعات المحاضرة:

Operational Amplifiers and their applications

Differentiator

الأساليب والأنشطة والوسائل التعليمية

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7- Differentiator

Its function is to provide an output voltage which is proportional to the rate of the change of
the input voltage. It is an inverse mathematical operation to that of an integrator. As shown in

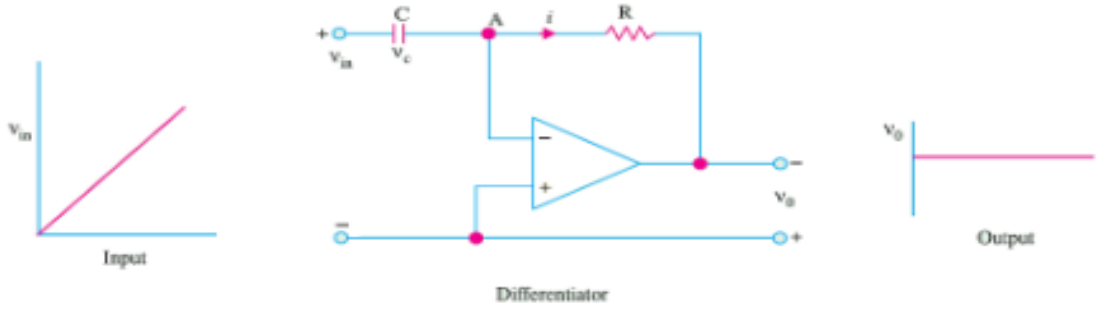

Fig. 11

Calculation:

The expression for the output signal of the inverting differentiator amplifier assuming the op amp is ideal can be derived as follows:

Taking point *A* as virtual ground, consequently, v_{in} appears across capacitor ($v_{in}=v_c$)

$$i = c\frac{dv_c}{dt} = -c\frac{dv_{in}}{dt}$$

$$v_o = -v_R = -iR = -c\frac{dv_{in}}{dt}R = -cR\frac{dv_{in}}{dt}$$

As seen, output voltage is proportional to the derivate of the input voltage, the constant of proportionality (*i.e.*, scale factor) being ($-RC$).

Example: The input to the differentiator circuit is a sinusoidal voltage of peak value of 5 mV and frequency 1 kHz. Find out the output if R = 1000 K and C = 1 μF.

Solution

The equation of the input voltage is v1 = 5 sin 2 π × 1000 t = 5 sin 2000 πt mV

scale factor = $CR = 10^{-6} \times 10^{5} = 0{\cdot}1$

$$v_0 = 0{\cdot}1\frac{d}{dt}(5\sin 2000\,\pi t) = (0{\cdot}5 \times 2000\,\pi)\cos$$

dt (5 sin 2000 πt) = (0·5 × 2000 π) cos 2000 πt = 1000 π cos 2000 πt mV

As seen, output is a cosinusoidal voltage of frequency 1 kHz and peak value 1000 π mV.

8- Comparator

It is a circuit which compares two signals or voltage levels. The circuit is the simple because it needs no additional external components shown in Fig. 12. If v1 and v2 are equal, then v0 should ideally be zero.

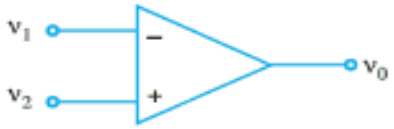

Fig. 12

Output of the comparator can be summarized as follows

If $V_1 > V_2$ then $V_o = -V_{cc}$ (Vsat)

If $V_1 < V_2$ then $V_o = V_{cc}$ (Vsat)

Application of comparator

1- Zero Crossing Detector

Comparator can be used as a zero crossing detector. A typical circuit for such a detector is shown below:

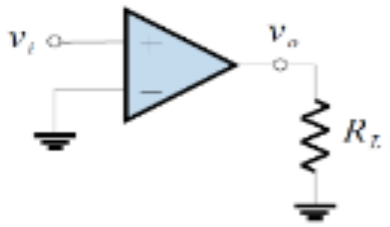

Fig. 14

During the positive half-cycle, the input voltage is positive, hence the output voltage is +*V*sat . During the negative half-cycle, the input voltage is negative, hence the output voltage is -*Vsat* . Thus the output voltage switches between +Vsat and -Vsat whenever the input signal crosses the zero level.

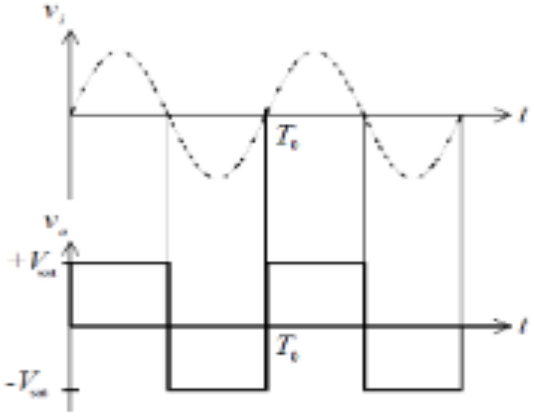

Fig. 15

Looking at the waveform shown above, we realize that a zero crossing detector can be used as a sine- to square-wave converter. This is an impractical circuit, since any noise on the input waveform near the zero crossings will cause multiple level transitions in the output signal (cause a comparator to erratically switch output states). In order to make the comparator less sensitive to noise, a comparator with positive feedback, called **hysteresis**, can be used. This comparator is called Schmitt trigger.

2- Output Bounding (or Voltage limiter)

In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than the saturation voltage. A single zener diode can be used, as shown in Fig. 16, to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other. This process of limiting the output range is called **bounding**.

The operation is as follows. Since the anode of the zener is connected to the inverting input, it is at virtual ground Therefore, when the output voltage reaches a positive value equal to the zener voltage, it limits at that value, as illustrated in Figure 17(a). When the output switches negative, the zener acts as a regular diode and becomes forward-biased at 0.7 V, limiting the negative output voltage to this value, as shown in part (b). Turning the zener around limits the output voltage in the opposite direction.

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اهداف المحاضرة:
ان يفهم الطالب Power Amplifier ويكون قادر على تمييزه

موضوعات المحاضرة:

Power Amplifier

.....

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة سؤال وجواب اختبار	• جهاز حاسوب • جهاز عرض • سبورة اوراق واقلام

المادة العلمية:

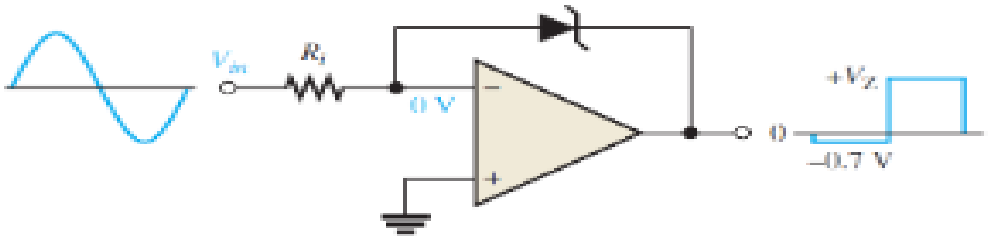

Fig. 17-(a) Bounded at a positive value

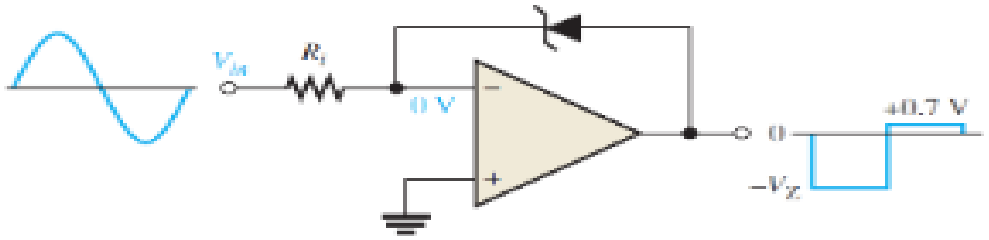

Fig. 17-(b) Bounded at a negative value

Two zener diode connected back to back with a comparator as in Fig. 18 to limit the output voltage to the zener voltage plus the voltage drop (0.7V) of the forward bias zener diode, both positively and negatively.

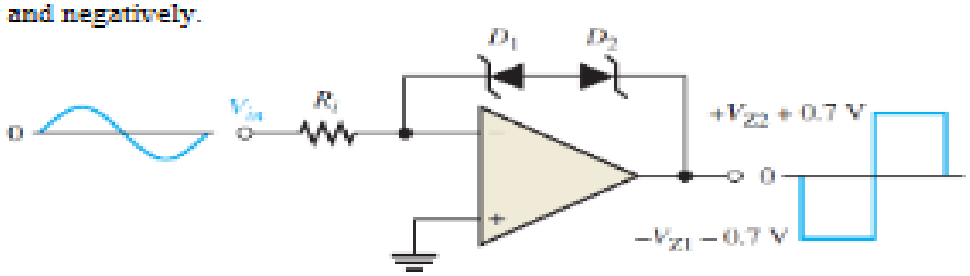

Fig. 18

9- Logarithmic and Antilog Amplifier

Log and antilog amplifiers are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. They are often used in high-frequency communication systems, including fiber optics, for processing wide dynamic range signals.

Note: The **logarithm** of a number is the power to which the base must be raised to get that number. A logarithmic (log) amplifier produces an output that is proportional to the logarithm of the input, and an antilogarithmic (antilog) amplifier takes the antilog or inverse log of the input.

a- Logarithmic Amplifier

The logarithmic amplifier is the use of a feedback-loop device that has an exponential terminal characteristic curve (diode or BJT transistor) which is characterized by

$$I_D = I_R(e^{V_D/V_T} - 1) \approx I_R e^{V_D/V_T} \quad \ldots\ldots(1)$$

Where I_R is reverse leakage current, I_D is the forward diode current, V_D is the forward diode voltage (approximately 0.7 V), V_T is the thermal voltage and is a constant equal to approximately 25 mV at 25C°.

12

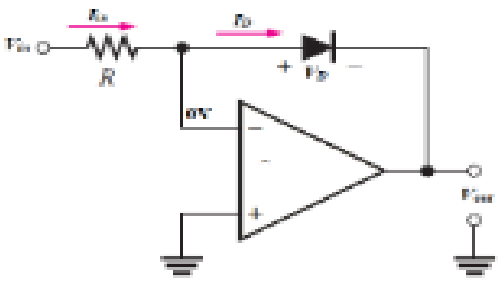

Fig. 19

An analysis of the circuit in Figure 19 is as follows, beginning with the facts that:

$$I_R = \frac{V_{in}}{R} = I_D \quad \ldots\ldots\ldots(2)$$

and $V_D = -V_{out}$ $\ldots\ldots\ldots(3)$

Substituting into the formula of eq. 1,

$$\frac{V_{in}}{R} = I_R e^{-V_{out}/V_T} \quad \Rightarrow \quad V_{in} = RI_R e^{-V_{out}/V_T}$$

Take the natural logarithm (ln) of both sides

$$\ln(V_{in}) = \ln(RI_R e^{-V_{out}/V_T}) \Rightarrow \ln(V_{in}) = \ln(RI_R) - \frac{V_{out}}{V_T} \quad \ldots\ldots\ldots(4)$$

$$V_{out} = V_T[\ln(RI_R) - \ln(V_{in})] = -V_T \ln\frac{V_{in}}{RI_R} \quad \ldots\ldots\ldots(5)$$

Under the condition that the term RI_R is negligible (which can be accomplished by controlling R so that $RI_R \approx 1$, where the factor I_R, is a constant for a given diode), then gives $V_{out} \approx -V_T \ln(V_{in})$.

Note: *ln* is the natural logarithm to the base *e*. A **natural logarithm** is the exponent to which the base *e* must be raised in order to equal a given quantity. Although eq. 5 will use natural logarithms in the formulas, each expression can be converted to a logarithm to the base 10(log10) using the relationship $\ln x = 2.3 \log 10x$.

Example: Determine the output voltage for the log amplifier in Fig. 19. Assume I_R = 50nA and R=100k.

Solution:

$$V_{OUT} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R}\right) = -(0.025\text{ V})\ln\left(\frac{2\text{ V}}{(50\text{ nA})(100\text{ k}\Omega)}\right)$$

$$= -(0.025\text{ V})\ln(400) = -(0.025\text{ V})(5.99) = \mathbf{-0.150\text{ V}}$$

Note1: The output voltage of the logarithmic amplifier is limited to a maximum value of approximately (-0.7V).

Note2: The input must be positive when the diode is connected in the direction shown in the Fig. 19. To handle negative inputs, the diode must be reversed.

Log Amplifier with a BJT

The base-emitter junction of a bipolar junction transistor exhibits the same type of logarithmic characteristic as a diode because it is also a *pn* junction. A log amplifier with a BJT connected in a common-base form in the feedback loop is shown in Figure 20. Notice that *Vout* with respect to ground is equal to $-V_{BE}$.

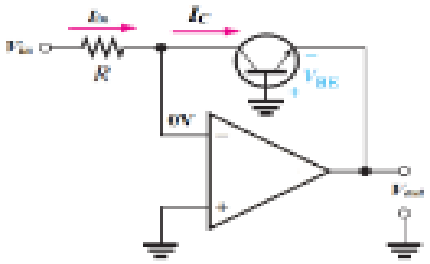

Fig. 20

The analysis for this circuit is the same as for the diode log amplifier except that V_{BE} replaces V_D, I_C replaces I_D and I_{EBO} replaces I_S. The expression for the V_{BE} versus I_C characteristic curve is

$$I_C = I_{EBO} e^{V_{BE}/V_T}$$

where I_{EBO} is the emitter-to-base leakage current. The expression for the output voltage is

$$V_{out} = -V_T \ln\left(\frac{V_{in}}{I_{EBO} R}\right)$$

b- Antilog Amplifier

The **antilogarithm** of a number is the result obtained when the base is raised to a power equal to the logarithm of that number. To get the antilogarithm, you must take the exponential of the logarithm (antilogarithm of $x = e^{\ln x}$).

An antilog amplifier is formed by connecting a transistor (or diode) as the input element as shown in Fig. 21. The exponential formula still applies to the base-emitter *pn* junction. The output voltage is determined by the current (equal to the collector current) through the feedback resistor.

$$V_{OUT} = -R_f I_C$$

The characteristic equation of the *pn* junction is

$$I_C = I_{EBO} e^{V_{BE}/V_T}$$

Substituting into the equation for V_{out}

$$V_{out} = -R_f I_{EBO} e^{V_{BE}/V_T}$$

As you can see in Fig. 21, $V_{in} = V_{BE}$

$$V_{out} = -R_f I_{EBO} e^{V_{in}/V_T}$$

The exponential term can be expressed as an antilogarithm as follows:

$$V_{out} = -R_f I_{EBO} \, antilog\left(\frac{V_{in}}{V_T}\right)$$

Where V_T is approximately 25 mV.

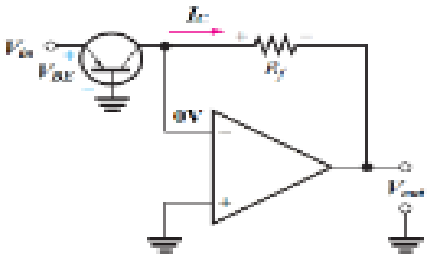

Fig. 21

الوحدة السادسة - المحاضرة التاسعة والعشرون - الزمن: 120 دقيقة

اهداف المحاضرة:

ان يفهم الطالب ماهي مقومات الدقة للمضخمات المستخدمة

موضوعات المحاضرة:

Power Amplifier
Precision Rectifiers

الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
1	• محاضرة • مناقشة سؤال وجواب اختبار	• جهاز حاسوب • جهاز عرض • سبورة اوراق واقلام

المادة العلمية:

2- Precision Rectifiers

Rectifier circuits can be implemented with silicon junction diodes. Recall that for the diode to conduct, the voltage across it must be ≈ 0.7 V. Therefore, a major limitation of these

circuits is that they cannot rectify voltages below about 0.7 V. In addition, since the input voltage has to rise to about 0.7 V before any appreciable change can be seen at the output, the

output is distorted

- half-wave rectifier (HWR) is a circuit that passes only the positive (or only the negative) portion of a wave, while blocking out the other portion. The transfer characteristic of the positive HWR is:

vO = vi for vi > 0 , vO = 0 for vi < 0.

- full-wave rectifier (FWR), besides passing the positive portion, inverts and then passes also

the negative portion. Its transfer characteristic is:

vO = vi for vi > 0 , vO = vi for vi < 0. or, more concisely, vO = |vi

Full-Wave Rectifiers

There are many configuration for achieving precision FWR. One of them is given in Fig. 29. Here op amp (OA1) provides inverting half-wave rectification, and op amp (OA2) sums v_I and the HWR output (v_{HW}) to give $v_O = -[(R_5/R_4)v_I + (R_5/R_3)v_{HW}]$.
Where $v_{HW} = -(R_2/R_1)v_I$ for $v_I > 0$, and $v_{HW} = 0$ for $v_I < 0$.

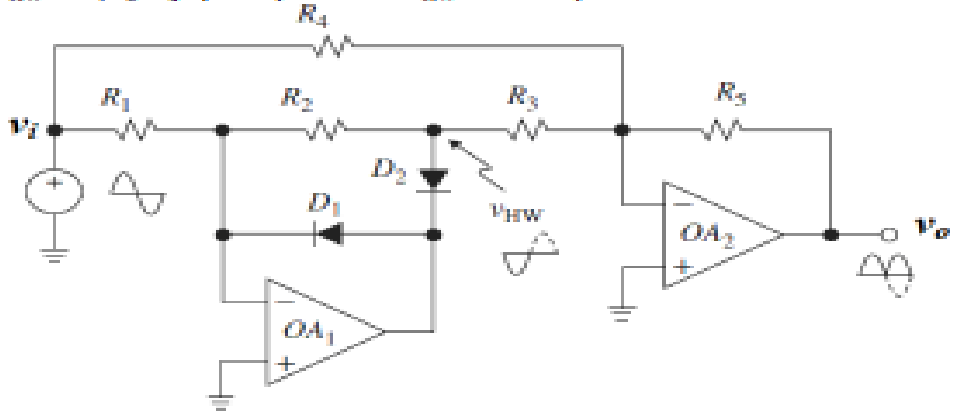

Fig. 29

i- Half-Wave Rectifiers

Figure 26 below shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an ideal op-amp.

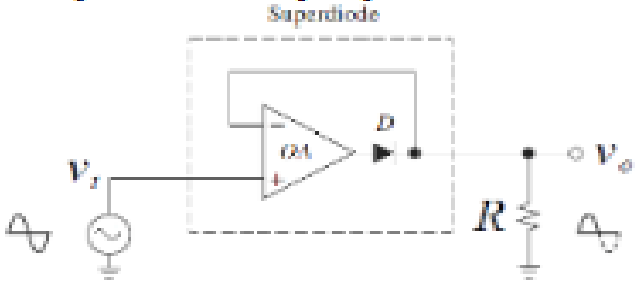

Fig. 26

The analysis of the circuit of Fig. 26 above is illustrated as below:

1- when input voltage is positive ($v_i > 0$), the op-amp output (v) will also positive, turning ON the diode and thus creating the negative-feedback path shown in Fig. 27-a. This allows op amp to operate as voltage follower and give $v_o = v_i$ (prove that). The output of the op amp (v) is a diode drop above v_o, ($v = v_o + V_{D(on)}$) $\approx v_o + 0.7$ V.

2- when input voltage is negative ($v_i < 0$): The op amp output (v) is negative, turning the diode OFF and thus causing the current through R to go to zero. Hence, $v_o = 0$. As shown in Fig. 27-b, the op amp is now operating in the open-loop mode.

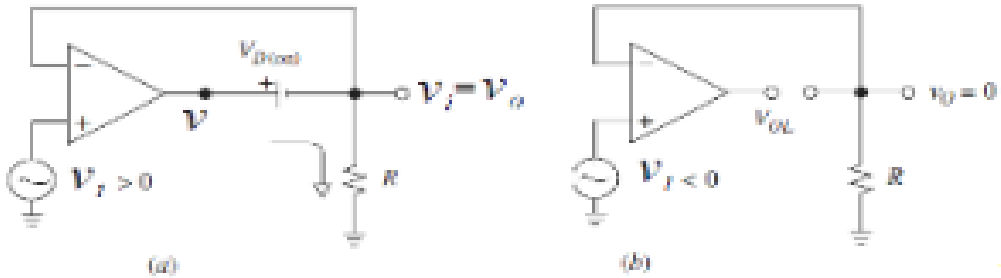

Fig. 27

A disadvantage of this circuit is that when v_i changes from positive to negative the op-amp will be saturated close to its negative supply rail. Thus, the op amp output may exhibit intolerable distortion. The improved HWR of Fig. 28 alleviates this inconvenience by using a second diode. Circuit operation is summarized as:

1- $v_i > 0$ ➔ $v_o = 0$. (positive input causes D_1 to conduct, thus creating a negative-feedback path around the op amp. By the virtual-ground, D_1 now clamps the op amp output at $v = -V_{D(on)} \approx -0.7$ V. Moreover, D_2 is OFF, so no current flows through R_2 and, hence, $v_o = 0$).

2- $v_i < 0$ ➔ $v_o = v_i$. (negative input causes the op amp output positive, thus turning D_2 ON. This creates an alternative negative-feedback path via D_2 and R_2. Clearly, D_1 is now OFF, so the op amp operate as inverting amplifier, i.e. $v_o = (-R_2/R_1)v_i$).

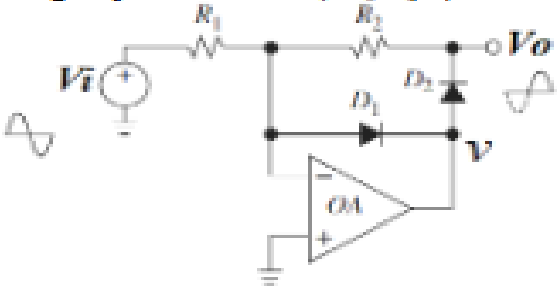

Fig. 28

Example1: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.30. Assume the maximum output levels of the op-amp are ± 12V.

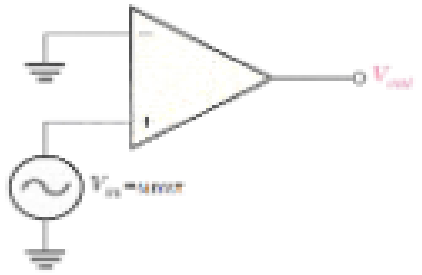

Fig.30

Solution:
When Vin > 0 ➔ Vout =+12 (maximum positive level)
When Vin > 0 ➔ Vout =-12 (maximum negative level)

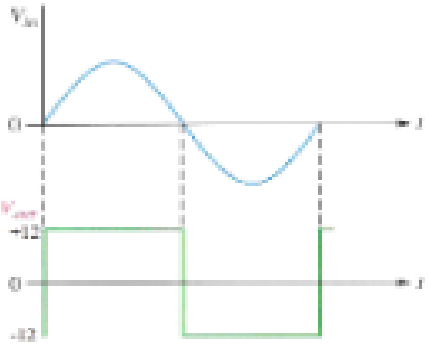

Fig. 40

Example2: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.41. Assume the maximum output levels of the op-amp are ±12V.

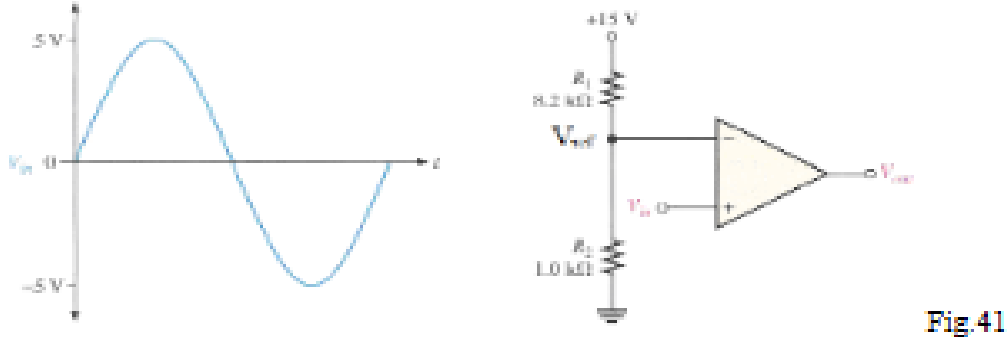

Fig.41

Solution:
The reference voltage (V_{REF}) is set by R_1 and R_2 (use voltage divider rule)

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V) = \frac{1.0\,\text{k}\Omega}{8.2\,\text{k}\Omega + 1.0\,\text{k}\Omega}(+15\,\text{V}) = 1.63\,\text{V}$$

As shown in Fig. 42, each time the input exceeds +1.63 V, the output voltage switches to its +12V level, and each time the input goes below +1.63 V, the output voltage switches to its -12V level.

الوحدة السادسة - المحاضرة الثلاثون - الزمن: 120 دقيقة

اهداف المحاضرة:

ان يفهم الطالب ويتعلم التحويل Digital to Analog conversion

موضوعات المحاضرة:

Power Amplifier
Digital to Analog conversion

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الأساليب والأنشطة والوسائل التعليمية

م	الأساليب والأنشطة التعليمية	الوسائل التعليمية
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المادة العلمية:

Digital to Analog conversion

It is an important interface process for converting digital signals to analog signals. An example is a voice signal that is digitized for storage, processing, or transmission and must be changed back into an approximation of the original audio signal in order to drive a speaker.
The $R/2R$ ladder is more commonly method used for D/A conversion because it requires only two resistor values as shown in Fig. 48 for four bits.

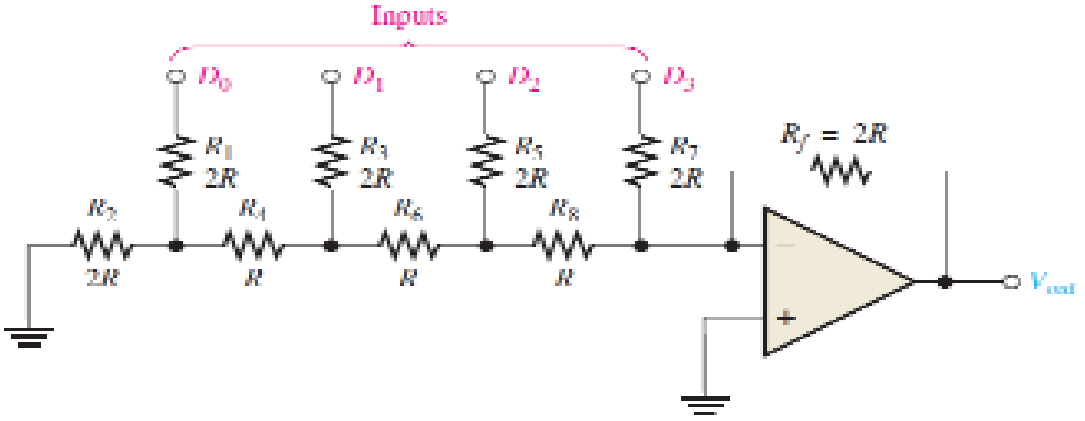
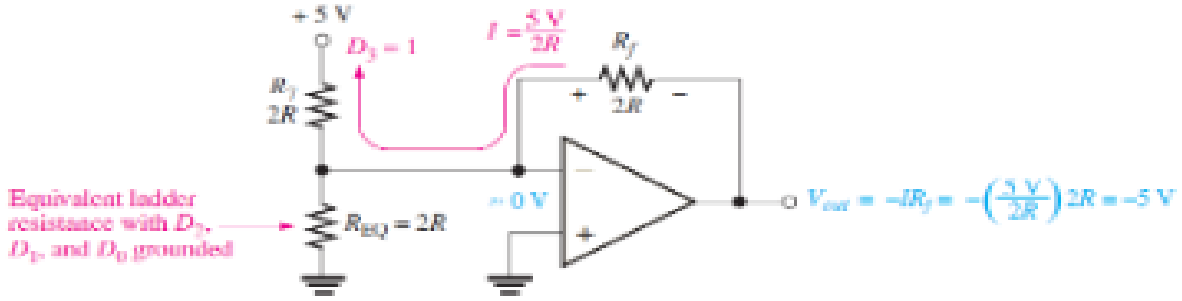


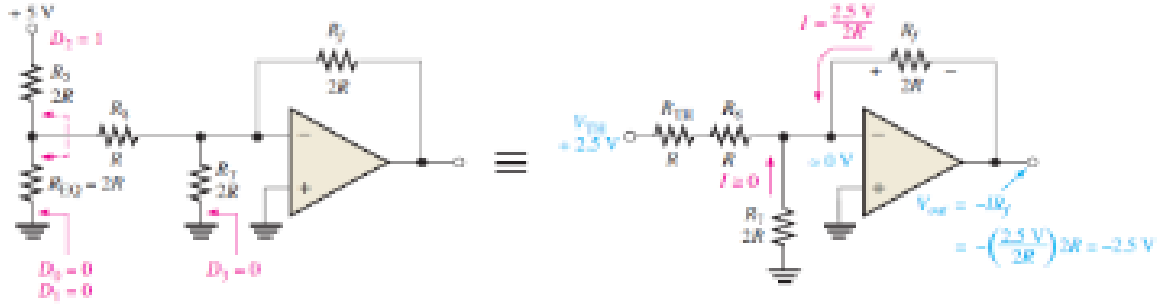
Fig. 48

Assume that the $D3$ input is HIGH (+5 V) and the others are LOW (ground, 0 V). This condition represents the binary number 1000. A circuit analysis will show that this reduces to the equivalent form shown in Fig. 49 (a).
Essentially no current goes through the $2R$ equivalent resistance (R_{EQ}) because the inverting input is at virtual ground. Thus, all of the current (I=5/2R) through $R7$ is also through Rf, and the output voltage is -5V.



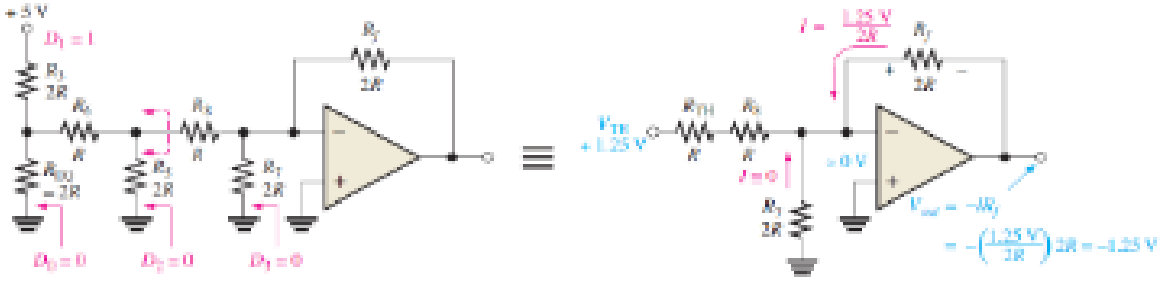
(a) Equivalent circuit for $D_3 = 1$, $D_2 = 0$, $D_1 = 0$, $D_0 = 0$

Figure (b) shows the equivalent circuit when the $D2$ input is at +5 V and the others are at ground. This condition represents 0100. If we thevenize looking from $R8$, we get 2.5 V in series with R, as shown. This results in a current through Rf of I= 2.5/2R, which gives an output voltage of -2.5V. Keep in mind that there is no current from the op-amp inverting input and that there is no current through $R7$ because it has 0 V across it, due to the virtual ground.



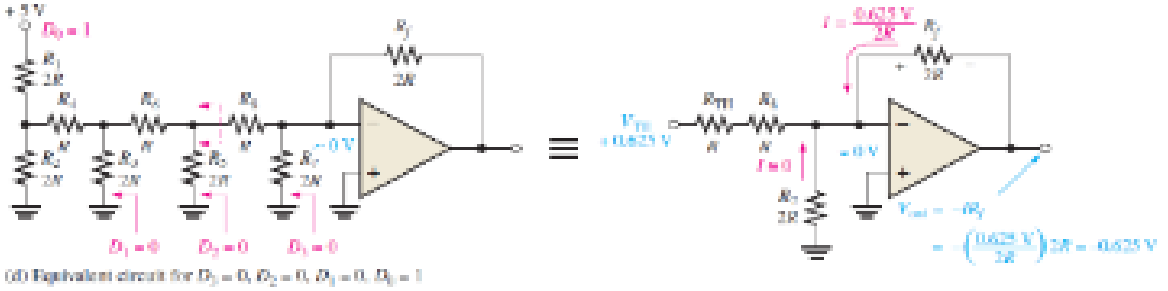
(b) Equivalent circuit for $D_3 = 0, D_2 = 1, D_1 = 0, D_0 = 0$

Figure (c) shows the equivalent circuit when the *D*1 input is at +5 V and the others are at ground. This condition represents 0010. Again thevenizing looking from *R*8, you get 1.25 V in series with *R* as shown. This results in a current through *Rf* of *I*= 1.25 V/2*R*, which gives an output voltage of -1.25.



(c) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 1, D_0 = 0$

In Fig. (d), the equivalent circuit representing the case where *D*0 is at +5 V and the other inputs are at ground is shown. This condition represents 0001. Thevenizing from *R*8 gives an equivalent of 0.625 V in series with *R* as shown. The resulting current through *Rf* is *I*=0.625V/2*R*, which gives an output voltage of -0.625 V.



(d) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 0, D_0 = 1$

Notice that each successively lower-weighted input produces an output voltage that is halved, so that the output voltage is proportional to the binary weight of the input bits.

In summary, We can prove that the equivalent analog voltage shown in Fig. 50 below is obtained from the relation:

$$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D + \dots}{2^n}$$

((The proof is left as an exercise))

Where (n) is the number of digital inputs.

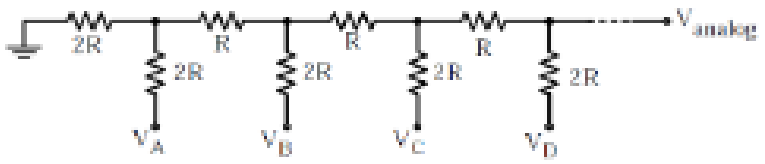


Fig.50

Figure 51 shows a four–bit R–2R ladder network and an op–amp connected to form a DAC. The op amp shown is an inverting amplifier and in this case the reference voltage (V_{ref}) should be negative so that the amplifier output will be positive. Alternately, a non–inverting op amp could be used with a positive value of (V_{ref})

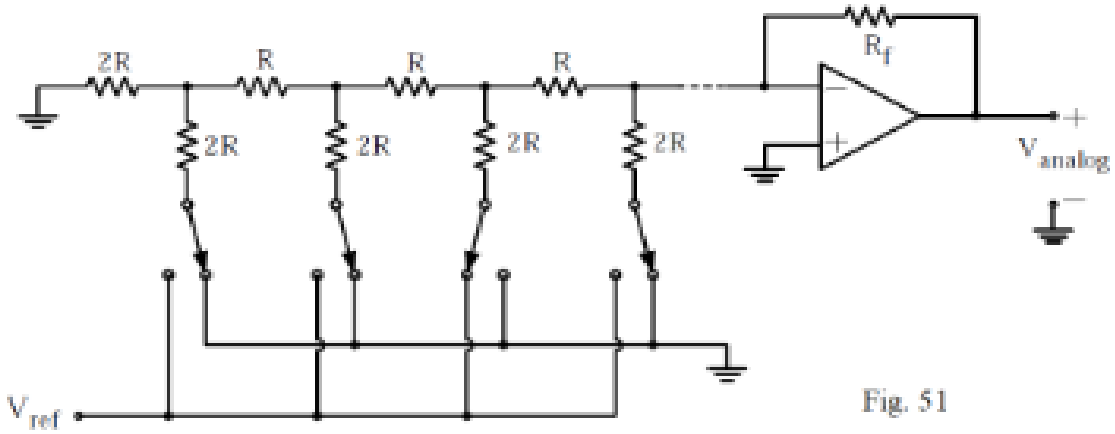


Fig. 51

Example: Figure 52 shows a four–bit DAC where all four switches are set at the ground level. Find the analog voltage value at the output of the unity gain amplifier for each of the sets of the switch positions shown in Table. Fill–in the right–most column with your answers.

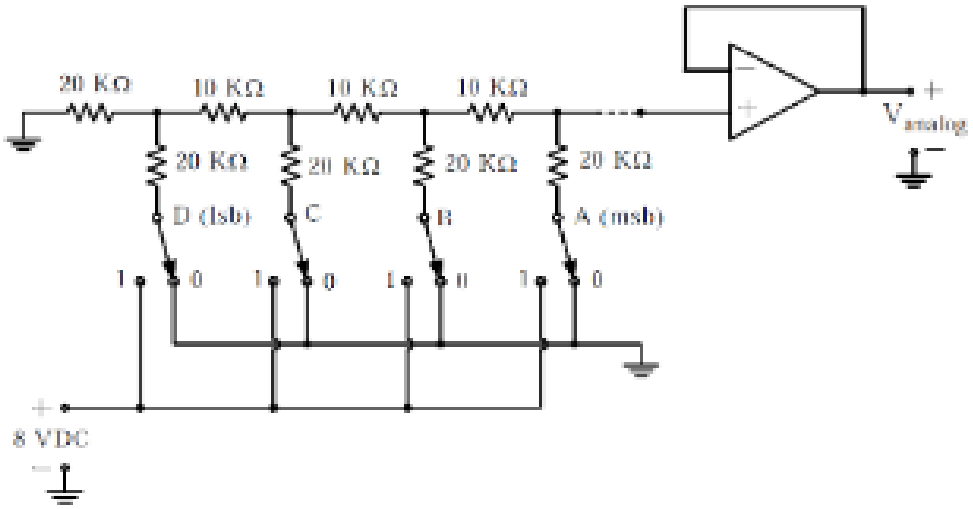


Fig. 52

	A 2^0	B 2^1	C 2^2	D 2^3	
(a)	1	1	1	1	
(b)	1	0	0	1	
(c)	1	0	1	0	
(d)	0	1	0	0	

Solution:

This is a 4−bit DAC and thus we have $n=2^4=16$ distinct binary values from 0000 to 1111 corresponding to decimals 0 through 15 respectively.

a. $V_{analog} = \frac{V_A+2V_B+4V_C+8V_D}{2^n} = \frac{1\times8+2\times8+4\times8+8\times8}{2^4} = 7.5\ V$

b. $V_{analog} = \frac{V_A+2V_B+4V_C+8V_D}{2^n} = \frac{1\times8+2\times0+4\times0+8\times8}{2^4} = 4.5\ V$

c. $V_{analog} = \frac{V_A+2V_B+4V_C+8V_D}{2^n} = \frac{1\times8+2\times0+4\times8+8\times0}{2^4} = 2.5\ V$

d. $V_{analog} = \frac{V_A+2V_B+4V_C+8V_D}{2^n} = \frac{1\times0+2\times8+4\times0+8\times0}{2^4} = 1.0\ V$

Based on these results, we can now fill−in the right−most column with the values we obtained, and we can plot the output versus inputs of the R−2R network for the voltage levels and as shown in Figure 53.

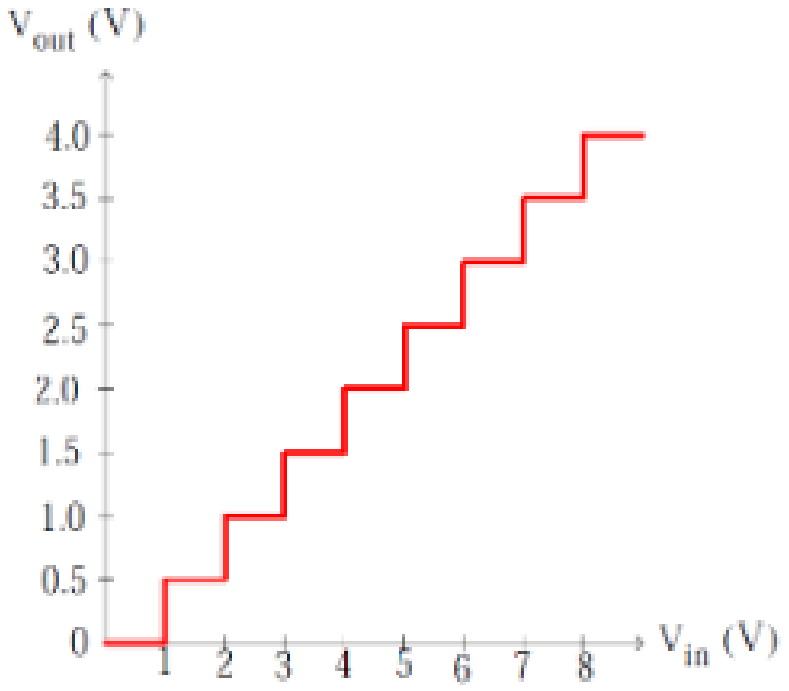


Fig.53